

ELECTRICAL CHARACTERISTICS

T_{MIN} to T_{MAX} @ V_{CC} = +5V ±5% unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V _{IL}			0.8	Volts	
V _{IH}	2.0			Volts	
LOGIC OUTPUTS					
V _{OL}			0.4	Volts	I _{OUT} = -3.2mA
V _{OH}	2.4			Volts	I _{OUT} = 1.0mA
RS-485 DRIVER					
TTL Input Levels					
V _{IL}			0.8	Volts	
V _{IH}	2.0			Volts	
Outputs					
HIGH Level Output			+6.0	Volts	
LOW level Output	-0.3			Volts	
Differential Output	±1.5		±5.0	Volts	R _L = 54Ω, C _L = 50pF
Balance			±0.2	Volts	V _T - V _r
Open Circuit Voltage			±6.0	Volts	
Output Current	28.0			mA	R _L = 54Ω
Short Circuit Current			±250	mA	Terminated in -7V to +12V
Transition Time			120	ns	Rise/fall time, 10%–90%
Maximum Transmission Rate	5			Mbps	R _L = 54Ω
Propagation Delay					
t _{PHL}			200	ns	R _L = 54Ω
t _{PLH}			200	ns	R _L = 54Ω
RS-485 RECEIVER					
TTL Output Levels					
V _{OL}			0.4	Volts	
V _{OH}	2.4			Volts	
Input					
HIGH Threshold	+0.2		+12.0	Volts	(a)-(b)
LOW Threshold	-7.0		-0.2	Volts	(a)-(b)
Common Mode Range	-7.0		+12.0	Volts	
HIGH Input Current					Refer to graph
LOW Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	Over -7V to +12V common mode range
Input Impedance	12			kΩ	
Maximum Transmission Rate	5			Mbps	
Propagation Delay					
t _{PHL}			200	ns	
t _{PLH}			200	ns	
V.35 DRIVER					
TTL Input Levels					
V _{IL}			0.8	Volts	
V _{IH}	2.0			Volts	
Outputs					
Differential Output	±0.44		±0.66	Volts	With termination network in Figure 6; R _L = 100Ω
Output Impedance	50		150	Ω	With termination network in Figure 6.
Short Circuit Impedance	135	150	165	Ω	With termination network in Figure 6.
Transition Time			40	ns	
Maximum Transmission Rate	5			Mbps	R _L = 100Ω
Propagation Delay					
t _{PHL}			200	ns	R _L = 100Ω
t _{PLH}			200	ns	R _L = 100Ω

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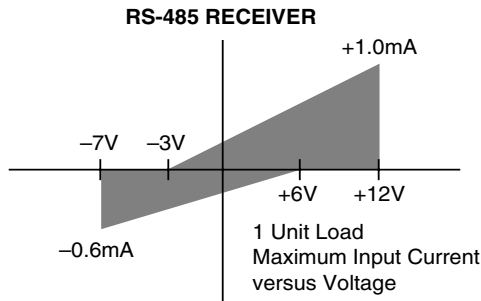
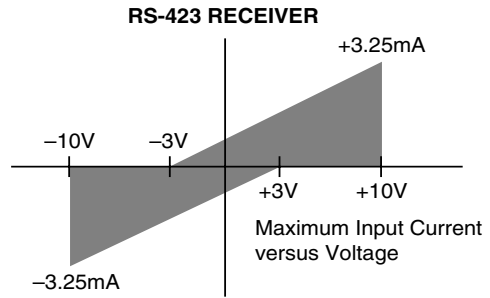
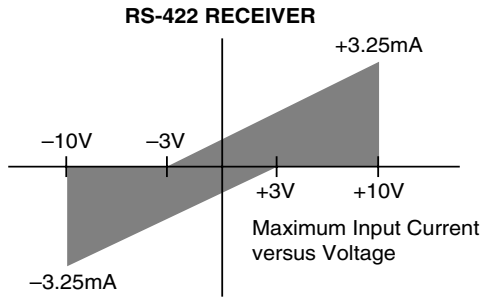
	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.35 RECEIVER					
TTL Output Levels					
V _{OL}			0.4	Volts	
V _{OH}	2.4			Volts	
Input					
Receiver Sensitivity		±0.2		Volts	
Input Impedance	90	100	110	Ω	With termination network in Figure 6. With termination network in Figure 6.
Short Circuit Impedance	135	150	165	Ω	
Maximum Transmission Rate	5			Mbps	
Propagation Delay					
t _{PHL}			200	ns	
t _{PLH}			200	ns	
RS-422 DRIVER					
TTL Input Levels					
V _{IL}			0.8	Volts	
V _{IH}	2.0			Volts	
Outputs					
Differential Output	±2.0		±5.0	Volts	R _L =100Ω
Open Circuit Voltage, V _O			±6.0	Volts	
Balance			±0.4	Volts	V _T - V _T
Offset			+3.0	Volts	
Short Circuit Current			±150	mA	V _{OUT} =0V
Power Off Current			±100	μA	V _{cc} = 0V, V _{out} = ±0.25V
Transition Time			60	ns	Rise/fall time, 10%-90%
Maximum Transmission Rate	5			Mbps	R _L =100Ω
Propagation Delay					
t _{PHL}			200	ns	R _L =100Ω
t _{PLH}			200	ns	R _L =100Ω
RS-422 RECEIVER					
TTL Output Levels					
V _{OL}			0.4	Volts	
V _{OH}	2.4			Volts	
Input					
HIGH Threshold	+0.2		+6.0	Volts	(a)-(b)
LOW Threshold	-6.0		-0.2	Volts	(a)-(b)
Common Mode Range	-7.0		+7.0	Volts	
HIGH Input Current					Refer to graph
LOW Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	V _{CM} =+7V to -7V
Input Impedance	4			kΩ	V _{CM} =+10V to -10V
Maximum Transmission Rate	5			Mbps	
Propagation Delay					
t _{PHL}			200	ns	
t _{PLH}			200	ns	
RS-232 DRIVER					
TTL Input Level					
V _{IL}			0.8	Volts	
V _{IH}	2.0			Volts	
Outputs					
HIGH Level Output	+5.0		+15	Volts	R _L =3kΩ, V _{IN} =0.8V, V _{cc} = 5V
LOW Level Output	-15.0		-5.0	Volts	R _L =3kΩ, V _{IN} =2.0V, V _{cc} = 5V
Open Circuit Voltage	-15		+15	Volts	
Short Circuit Current			±100	mA	V _{OUT} =0V
Power Off Impedance	300			Ω	V _{cc} = 0V, V _{out} = ±2.0V

ELECTRICAL CHARACTERISTICS

T_{MIN} to T_{MAX} @ V_{CC} = +5V ±5% unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Slew Rate			30	V/μs	R _L =3kΩ, C _L =15pF
Transition Time			1.56	μs	R _L =3kΩ, C _L =2500pF
Maximum Transmission Rate	120			kbps	R _L =3kΩ, C _L =2500pF
Propagation Delay					
t _{PHL}		2	8	μs	R _L =3kΩ
t _{PLH}		2	8	μs	R _L =3kΩ
RS-232 RECEIVER					
TTL Output Levels					
V _{OL}	2.4		0.4	Volts	
V _{OH}				Volts	
Input					
HIGH Threshold		1.7	2.4	Volts	
LOW Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias			+2.0	Volts	
Input Impedance	3	5	7	kΩ	V _{IN} =+15V to -15V
Maximum Transmission Rate	120			kbps	
Propagation Delay					
t _{PHL}			1	μs	
t _{PLH}			1	μs	
RS-423 DRIVER					
TTL Input Levels					
V _{IL}	2.0		0.8	Volts	
V _{IH}				Volts	
Output					
Open Circuit Voltage	±4.0		±10.0	Volts	
HIGH Level Output	+3.6		+6.0	Volts	R _L =550Ω
LOW Level Output	-6.0		-3.6	Volts	R _L =550Ω
Short Circuit Current			±150	mA	V _{OUT} =0V
Power Off Current			±100	μA	V _{CC} = 0V, V _{out} = ±0.25V
Transition Time	0.8		2.4	μs	Rise/fall time, 10-90%
Maximum Transmission Rate	120			kbps	R _L =550Ω
Propagation Delay					
t _{PHL}		2	8	μs	R _L =550Ω
t _{PLH}		2	8	μs	R _L =550Ω
RS-423 RECEIVER					
TTL Output Levels					
V _{OL}	2.4		0.4	Volts	
V _{OH}				Volts	
Input					
HIGH Threshold	+0.2		+7.0	Volts	
LOW Threshold	-7.0		-0.2	Volts	
HIGH Input Current					
LOW Input Current					
Receiver Sensitivity			±0.2	Volts	Refer to graph
Input Impedance	4			kΩ	Refer to graph
Maximum Transmission Rate	120			kbps	V _{CM} = +7V to -7V
Propagation Delay					V _{IN} = +10V to -10V
t _{PHL}			1	μs	
t _{PLH}			1	μs	
POWER REQUIREMENTS					
V _{CC}	4.75		5.25	Volts	
I _{CC}		20	30	mA	V _{CC} =5V; no interface selected
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		+70	°C	
Storage Temperature Range	-65		+150	°C	
Package	80-pin QFP				

RECEIVER INPUT GRAPHS



POWER MATRIX

Typical @ 25°C and $V_{cc} = +5V$ unless otherwise noted. Input is applied to one driver.

Mode	Open Input	Input to 5V	Input to GND	AC Signal to Input	Input to 5V with Load	Input to GND with Load	AC Signal with Load	Conditions
V.35	47.0mA	48.8mA	47.3mA	54.5mA	104.2mA	100.9mA	100.9mA	With external termination resistor network; Input @ 60kHz, Load is 3kΩ & 2500pF for RS-232 and 100Ω for V.35
RS-232	35.4mA	37.8mA	35.2mA	43.6mA	54.1mA	57.1mA	55.9mA	Input @ 60kHz Load is 3kΩ & 2500pF for RS-232.
RS-422	25.8mA	31.4mA	25.8mA	27.5mA	140.2mA	135.9mA	145.2mA	Input @ 2.5MHz Load is 100Ω.
RS-485	33.4mA	37.91mA	33.51mA	34.81mA	200.3mA	194.8mA	203.3mA	Input @ 2.5MHz Load is 54Ω.
RS-449	37.8mA	40.3mA	41.1mA	42.9mA	142.3mA	138.8mA	147.4mA	Input @ 60kHz Load is 100Ω for RS-422 450Ω for RS-423
EIA-530	45.2mA	48.1mA	44.4mA	50.3mA	148.9mA	145.7mA	147.3mA	Input @ 60kHz Load is 100Ω for RS-422 450Ω for RS-423

OTHER AC CHARACTERISTICS

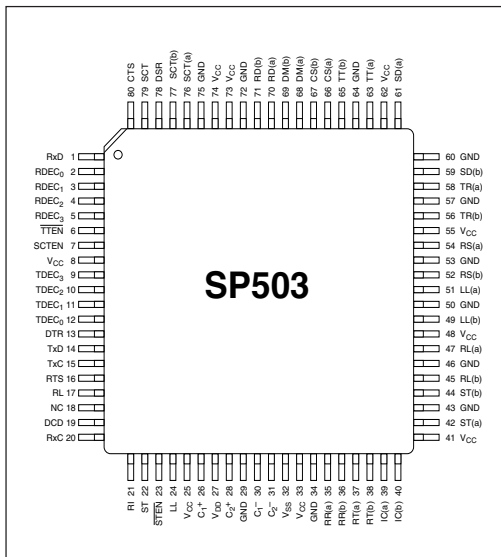
(Typical @ 25°C and nominal supply voltages unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DELAY TIME FROM ENABLE MODE TO TRI-STATE MODE					
SINGLE-ENDED MODE (RS-232, RS-423)					
t_{pZL} ; Enable to Output LOW		190		ns	3k Ω pull-up to output
t_{pZH} ; Enable to Output HIGH		130		ns	3k Ω pull-down to output
t_{pLZ} ; Disable from Output LOW		270		ns	5V to input
t_{pHZ} ; Disable from Output HIGH		400		ns	GND to input
DIFFERENTIAL MODE (RS-422, RS-485, V.35)					
t_{pZL} ; Enable to Output LOW		100		ns	3k Ω pull-up to output
t_{pZH} ; Enable to Output HIGH		100		ns	3k Ω pull-down to output
t_{pLZ} ; Disable from Output LOW		130		ns	5V to input
t_{pHZ} ; Disable from Output HIGH		140		ns	GND to input

Notes:

1. Measured from 2.5V of R_{IN} to 2.5V of R_{OUT} .
2. Measured from one-half of R_{IN} to 2.5V of R_{OUT} .
3. Measured from 1.5V of T_{IN} to one-half of T_{OUT} .
4. Measured from 2.5V of R_O to 0V of A and B.

PINOUT...



Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxC

Pin 65 — TT(b) — Analog Out — Terminal Timing, non-inverted; sourced from TxC.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

PIN ASSIGNMENTS...

CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; TTL input for TT driver outputs.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for SCT.

Pin 77 — SCT(b) — Serial Clock Transmit; analog input, non-inverted; source for SCT

Pin 79 — SCT — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 19 — DCD — Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring In; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a) — Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b) — Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a) — Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b) — Incoming Call; analog input, non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49 — LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a) — Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b) — Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a) — Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b) — Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR — Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.

Pin 80 — CTS — Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2–5 — RDEC₀ – RDEC₃ — Receiver decode register; configures receiver modes; TTL inputs.

Pin 6 — $\overline{\text{TTEN}}$ — Enables TT driver, active low; TTL input.

Pin 7 — SCTEN — Enables SCT receiver; active high; TTL input.

Pins 12–9 — TDEC₀ – TDEC₃ — Transmitter decode register; configures transmitter modes; TTL inputs.

Pin 23 — $\overline{\text{STEN}}$ — Enables ST driver; active low; TTL input.

POWER SUPPLIES

Pins 8, 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capacitor size is 22 μ F, 16V.

Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS} . Suggested capacitor size is 22 μ F, 16V.

Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^- . Suggested capacitor size is 22 μ F, 16V.

Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^- . Suggested capacitor size is 22 μ F, 16V.

NOTE: NC pins should be left floating; internal signals may be present.

FEATURES...

The **SP503** is a highly integrated serial transceiver that allows software control of its interface modes. The **SP503** offers hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-449, RS-485, V.35, and EIA-530. The interface mode selection is done via an 8-bit switch; four (4) bits control the drivers and four (4) bits control the receivers. The **SP503** is fabricated using low-power BiCMOS process technology, and incorporates a **Sipex** patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80-pin Quad FlatPack package.

The **SP503** is ideally suited for wide area network connectivity based on the interface modes offered and the driver and receiver configurations. The **SP503** has seven (7) independent drivers and seven (7) independent receivers. The seventh driver of the **SP503** allows it to support applications which require two separate clock outputs making it ideal for DCE applications.

THEORY OF OPERATION

The **SP503** is made up of four separate circuit blocks — the charge pump, drivers, receivers, and decoder. Each of these circuit blocks is described in more detail below.

Charge-Pump

The charge pump is a **Sipex** patented design (5,306,954) and uses a unique approach com-

pared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. *Figure 3(a)* shows the waveform found on the positive side of capacitor C_2 , and *Figure 3(b)* shows the negative side of capacitor C_2 . There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^- is then switched to ground and the charge on C_1^- is transferred to C_2^- . Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated -10V to C_3 . Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces -5V in the negative terminal of C_1 , which is applied to the negative side of capacitor C_2 . Since C_2^+ is at +5V, the voltage potential across C_2 is 10V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated 10V across C_2 to C_4 , the V_{DD} storage capacitor. Again,

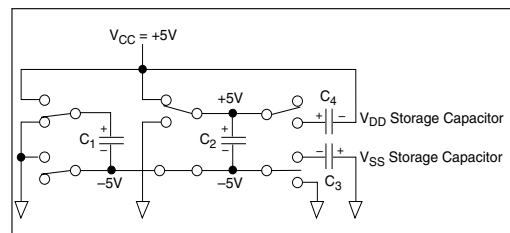


Figure 1. Charge Pump Phase 1.

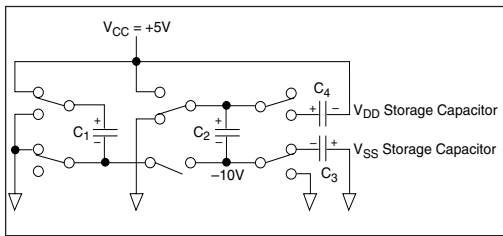


Figure 2. Charge Pump Phase 2.

simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V^+ and V^- are separately generated from V_{CC} in a no-load condition, V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 22 μ F with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V^+ and V^- pins. The value of the external supply voltages must be no greater than $\pm 10V$. The current drain for the $\pm 10V$ supplies is used for RS-232,

and RS-423 drivers. For the RS-232 driver, the current requirement will be 3.5mA per driver, and for the RS-423 driver, the worst case current drain will be 11mA per driver. The external power supplies should provide a power supply sequence of : +10V, then +5V, followed by -10V.

Drivers

The **SP503** has seven (7) independent drivers, two of which have separate active-low tri-state controls. If a half-duplex channel is required, this can be achieved with external connections.

Control for the mode selection is done via a four-bit control word. The **SP503** does not have a latch; the control word must be externally latched either high or low to write the appropriate code into the **SP503**. The drivers are pre-arranged such that for each mode of operation the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. *Table 1* shows a summary of the electrical characteristics of the drivers in the different interface modes. Unused driver inputs can be left floating; however, to ensure a desired state with no input signal, pull-up resistors to +5V or pull-down resistors to ground are suggested. Since the driver inputs are both TTL or CMOS compatible, any value resistor less than 100k Ω will suffice.

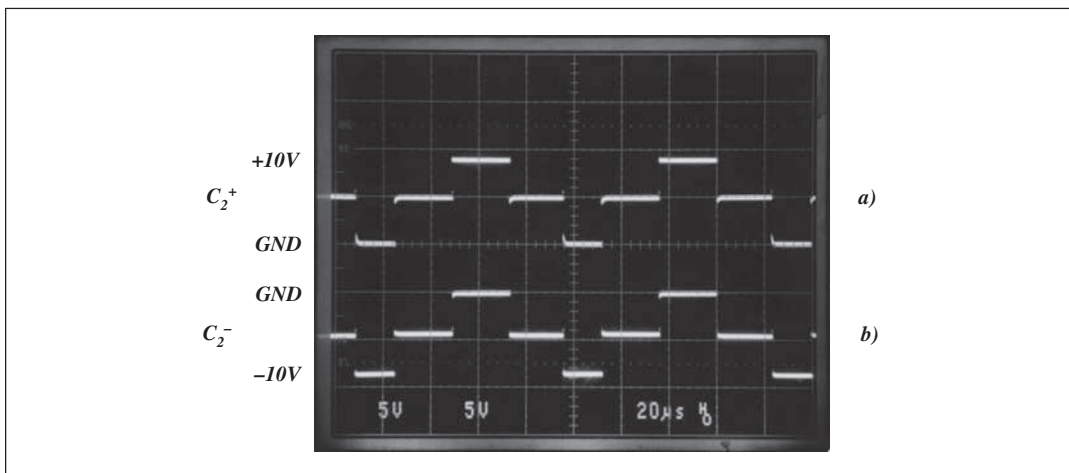


Figure 3. Charge Pump Waveforms

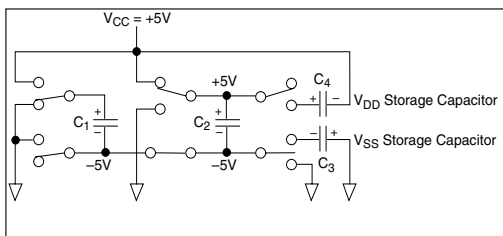


Figure 4. Charge Pump Phase 3.

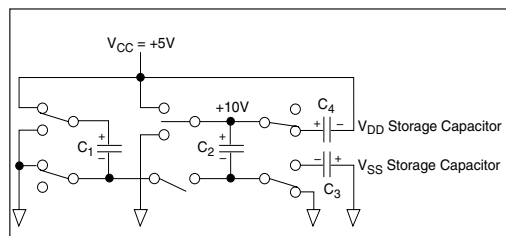


Figure 5. Charge Pump Phase 4.

There are three basic types of driver circuits — RS-232, RS-423, and RS-485. The RS-232 drivers output a minimum of $\pm 5V$ level single-ended signals (with $3k\Omega$ and $2500pF$ loading), and can operate up to 120kbps. The RS-232 drivers are used in RS-232 mode for all signals, and also in V.35 mode where they are used as the control line signals.

The RS-423 drivers output a minimum of $\pm 3.6V$ level single-ended signals (with 450Ω loading) and can operate up to 120kbps. Open circuit V_{OL} and V_{OH} measurements may exceed the $\pm 6V$ limitation of RS-423. The RS-423 drivers are used in RS-449 and EIA-530 modes as RL and LL outputs.

The third type of driver supports RS-485, which is a differential signal that can maintain $\pm 1.5V$ differential output levels with a worst case load of 54Ω . The signal levels and drive capability of

the RS-485 drivers allow the drivers to also support RS-422 requirements of $\pm 2V$ differential output levels with 100Ω loads. The RS-422 drivers are used in RS-449 and EIA-530 modes as clock, data, and some control line signals.

The RS-485-type drivers are also used in the V.35 mode. V.35 levels require $\pm 0.55V$ signals with a load of 100Ω . In order to meet the voltage requirements of V.35, external series resistors with source impedance termination resistors must be implemented to voltage divide the driver outputs from 0 to +5V to 0 to +0.55V. Figure 6 shows the values of the resistor network and how to connect them. The termination network also achieves the 50Ω to 150Ω source impedance for V.35. For applications that require V.11 signals for clock and data instead of V.35 levels, omit the external termination networks. All of the differential drivers, RS-485, RS-422, and V.35 can operate up to 5Mbps.

Pin Label	Mode:	RS-232	V.35	RS-422	RS-485	RS-449	EIA-530
TDEC ₃ -TDEC ₀	0000	0010	1110	0100	0101	1100	1101
SD(a)	tri-state	RS-232	V.35-	RS-422-	RS-485-	RS-422-	RS-422-
SD(b)	tri-state	tri-state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
TR(a)	tri-state	RS-232	RS-232	RS-422-	RS-485-	RS-422-	RS-422-
TR(b)	tri-state	tri-state	tri-state	RS-422+	RS-485+	RS-422+	RS-422+
RS(a)	tri-state	RS-232	RS-232	RS-422-	RS-485-	RS-422-	RS-422-
RS(b)	tri-state	tri-state	tri-state	RS-422+	RS-485+	RS-422+	RS-422+
RL(a)	tri-state	RS-232	RS-232	RS-422-	RS-485-	RS-423	RS-423
RL(b)	tri-state	tri-state	tri-state	RS-422+	RS-485+	tri-state	tri-state
LL(a)	tri-state	RS-232	RS-232	RS-422-	RS-485-	RS-423	RS-423
LL(b)	tri-state	tri-state	tri-state	RS-422+	RS-485+	tri-state	tri-state
ST(a)	tri-state	RS-232	V.35-	RS-422-	RS-485-	RS-422-	RS-422-
ST(b)	tri-state	tri-state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
TT(a)	tri-state	RS-232	V.35-	RS-422-	RS-485-	RS-422-	RS-422-
TT(b)	tri-state	tri-state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+

Table 1. SP503 Drivers

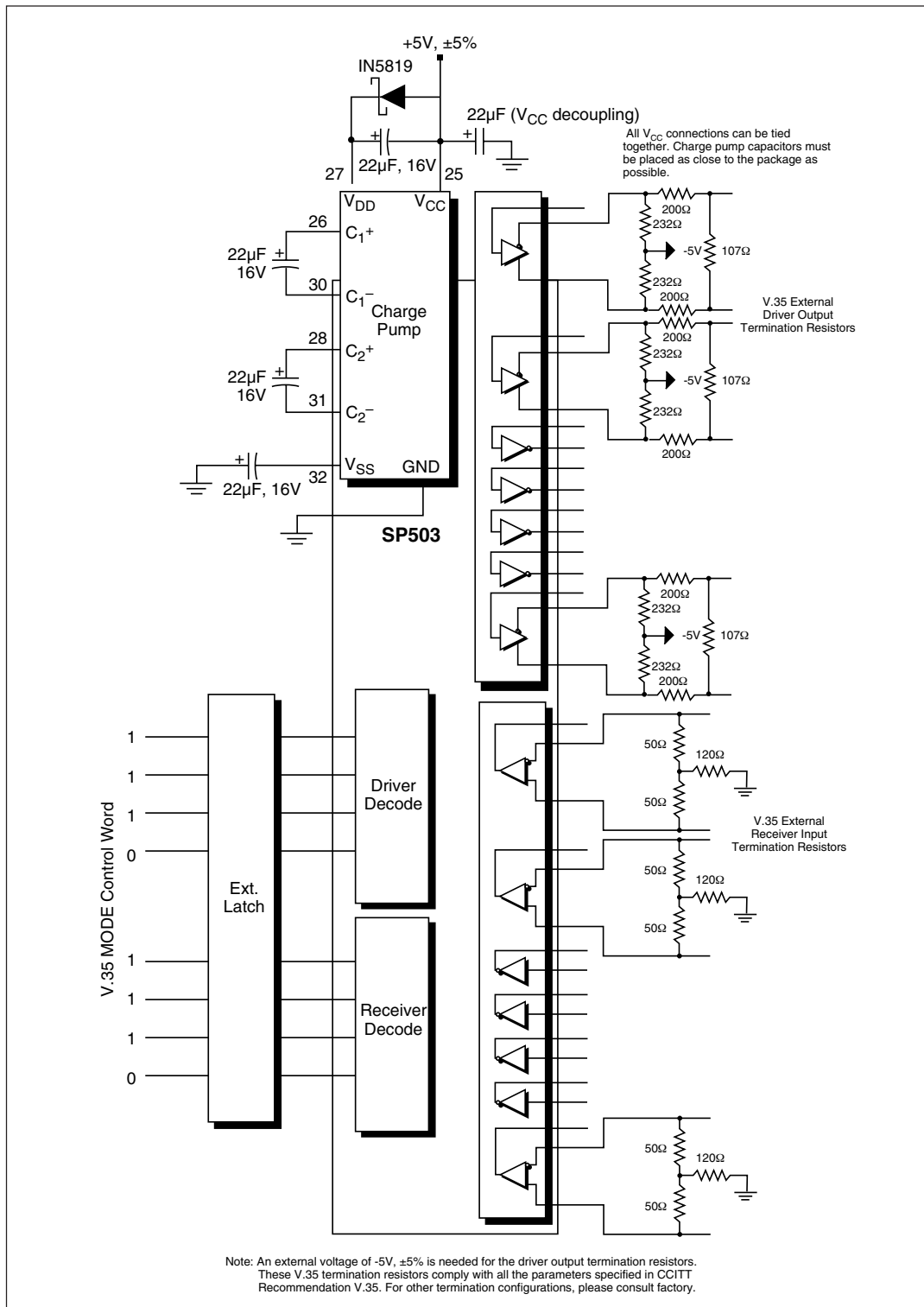


Figure 6. Typical Operating Circuit

Receivers

The **SP503** has seven (7) independent receivers which can be programmed for six (6) different interface modes. One of the seven (7) receivers (SCT) has an active-high enable control, as shown in the Mode Diagrams.

Control for the mode selection is done via a 4-bit control word that is independent from the driver control word. The coding for the drivers and receivers is identical. Therefore, if the modes for the drivers and receivers are supposed to be identical in the application, the control lines can be tied together.

Like the drivers, the receivers are pre-arranged for the specific requirements of the interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line receivers. *Table 2* shows a summary of the electrical characteristics of the receivers in the different interface modes. Unused receiver inputs can be left floating without causing oscillation. To ensure a desired state of the receiver output, a pull-up resistor of 100k Ω to +5V should be connected to the inverting input for a logic low, or the non-inverting input for a logic high. For single-ended receivers, a pull-down resistor to ground of 5k Ω is internally connected, which will ensure a logic high output.

There are three basic types of receivers — RS-232, RS-423, and RS-485. The RS-232 receiver is a single-ended input with a threshold of 0.8V to 2.4V. The RS-232 receiver has an operating voltage range of $\pm 15V$ and can receive signals up to 120kbps. RS-232 receivers are used in RS-232 mode for all signal types, and in V.35 mode for control line signals.

The RS-423 receivers are also single-ended but have an input threshold as low as $\pm 200mV$. The input impedance is guaranteed to be greater than 4k Ω , with an operating voltage range of $\pm 7V$. The RS-423 receivers can operate up to 120kbps. RS-423 receivers are used for the IC signal in RS-449 and EIA-530 modes, as shown in *Table 2*.

The third type of receiver supports RS-485, which is a differential interface mode. The RS-485 receiver has an input impedance of 15k Ω and a differential threshold of $\pm 200mV$. Since the characteristics of an RS-422 receiver are actually subsets of RS-485, the receivers for RS-422 requirements are identical to the RS-485 receivers. RS-422 receivers are used in RS-449 and EIA-530 for receiving clock, data, and some control line signals. The RS-485 receivers are also used for the V.35 mode. V.35 levels require the $\pm 0.55V$ signals with a load of 100 Ω . In order to meet the V.35 input impedance of 100 Ω , the external termination network of *Figure 6* must be applied. The threshold of the V.35 receiver is $\pm 200mV$. The V.35 receivers

Pin Label	Mode:	RS-232	V.35	RS-422	RS-485	RS-449	EIA-530
RDEC _s -RDEC _o	0000	0010	1110	0100	0101	1100	1101
RD(a)	Undefined	RS-232	V.35-	RS-422-	RS-485-	RS-422-	RS-422-
RD(b)	Undefined	15k Ω to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
RT(a)	Undefined	RS-232	V.35-	RS-422-	RS-485-	RS-422-	RS-422-
RT(b)	Undefined	15k Ω to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
CS(a)	Undefined	RS-232	RS-232	RS-422-	RS-485-	RS-422-	RS-422-
CS(b)	Undefined	15k Ω to GND	15K Ω to GND	RS-422+	RS-485+	RS-422+	RS-422+
DM(a)	Undefined	RS-232	RS-232	RS-422-	RS-485-	RS-422-	RS-422-
DM(b)	Undefined	15k Ω to GND	15K Ω to GND	RS-422+	RS-485+	RS-422+	RS-422+
RR(a)	Undefined	RS-232	RS-232	RS-422-	RS-485-	RS-422-	RS-422-
RR(b)	Undefined	15k Ω to GND	15K Ω to GND	RS-422+	RS-485+	RS-422+	RS-422+
IC(a)	Undefined	RS-232	RS-232	RS-422-	RS-485-	RS-423	RS-423
IC(b)	Undefined	15k Ω to GND	15K Ω to GND	RS-422+	RS-485+	15K Ω to GND	15K Ω to GND
SCT(a)	Undefined	RS-232	V.35-	RS-422-	RS-485-	RS-422-	RS-422-
SCT(b)	Undefined	15k Ω to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+

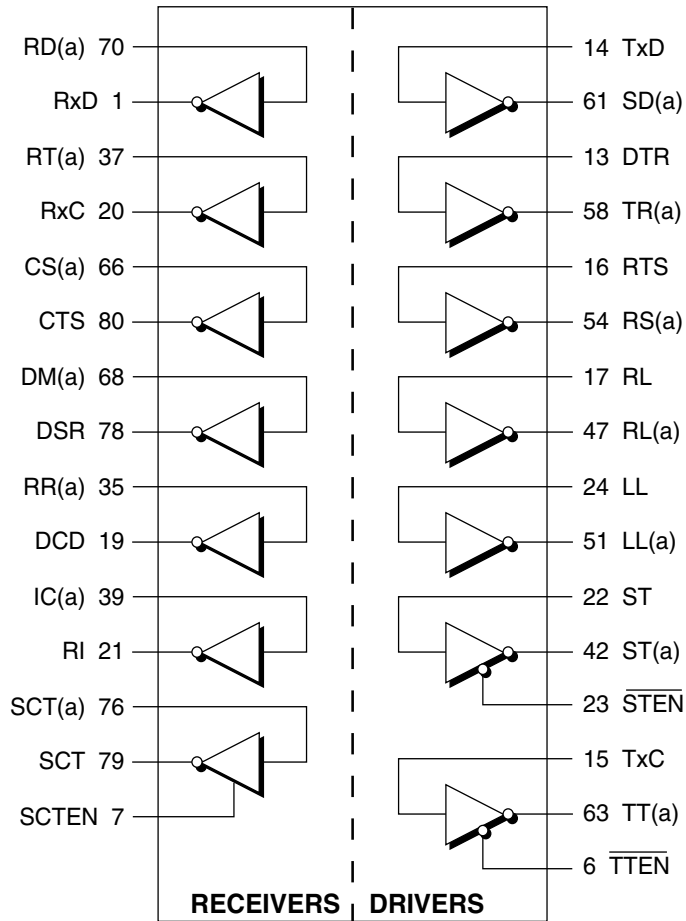
Table 2. SP503 Receivers

can operate up to 5Mbps. All of the differential receivers can receive data up to 5Mbps.

Decoder

The **SP503** has the ability to change the interface mode of the drivers or receivers via an 8-bit switch. The decoder for the drivers and receivers is not latched; it is merely a combinational logic switch. The codes shown in *Tables 1 and 2* are the only specified, valid modes for the **SP503**. Undefined codes may represent other interface modes not specified or random outputs (consult the factory for more information). The drivers are controlled with the data bits labeled $TDEC_3$ – $TDEC_0$. The drivers can be put into tri-state mode by writing 0000 to the driver decode switch. The receivers are controlled with data bits $RDEC_3$ – $RDEC_0$; the code 0000 written to the receivers will place the outputs in an undetermined state. All receivers, with the exception of SCT, do not have tri-state capability; the outputs will either be HIGH or LOW depending upon the state of the receiver input.

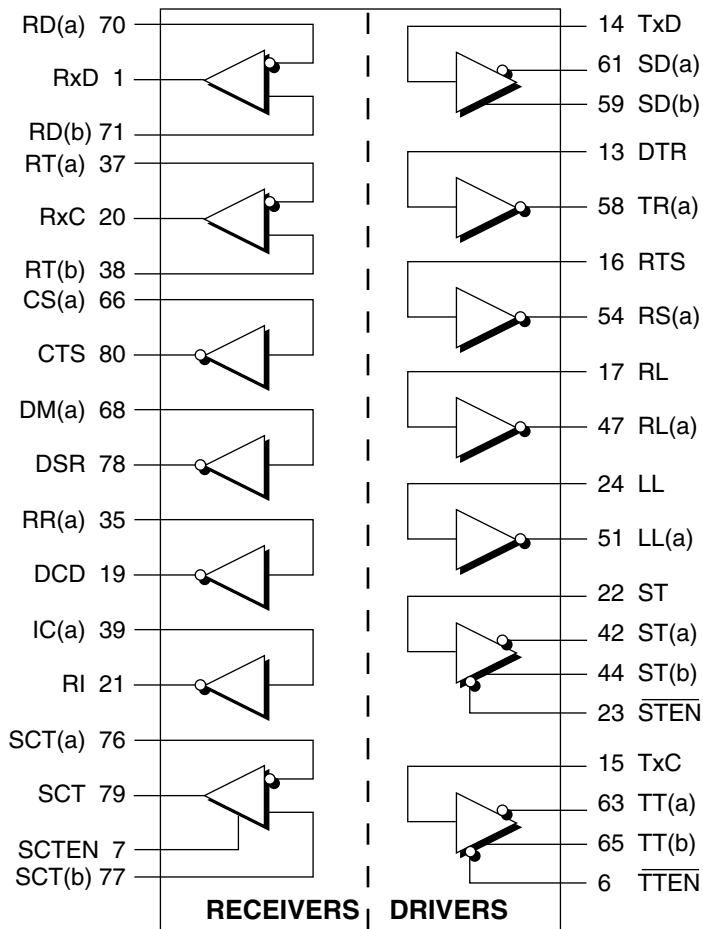
MODE: RS-232							
DRIVER				RECEIVER			
TDEC ₃	TDEC ₂	TDEC ₁	TDEC ₀	RDEC ₃	RDEC ₂	RDEC ₁	RDEC ₀
0	0	1	0	0	0	1	0



$\overline{\text{STEN}}$	ST	$\overline{\text{TTEN}}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 7. Mode Diagram — RS-232

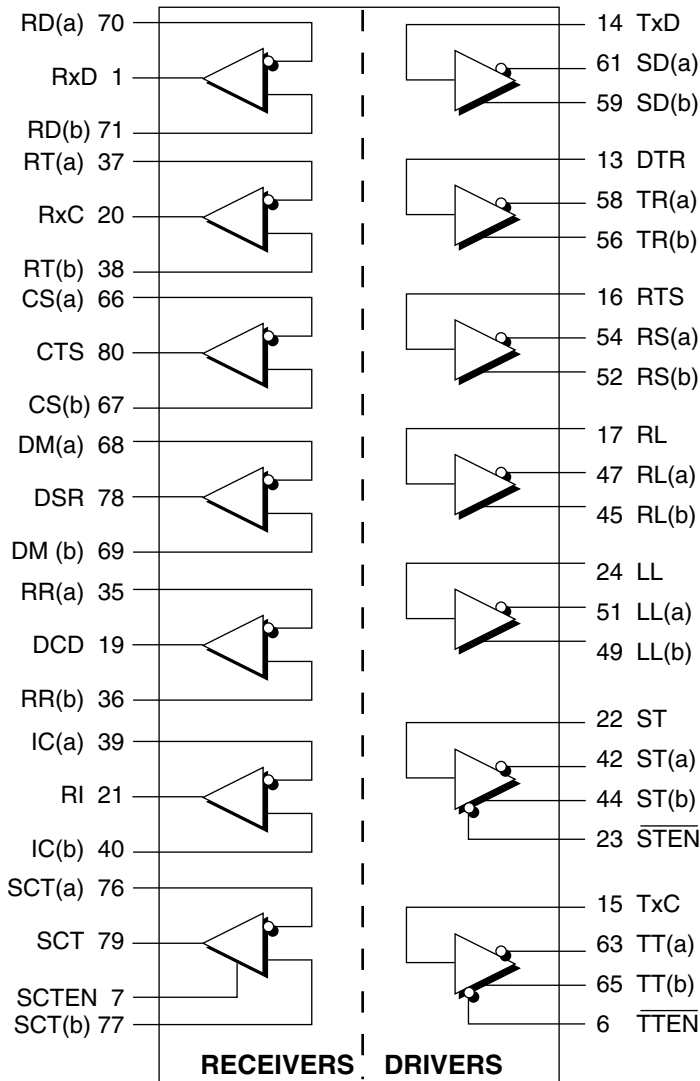
MODE: V.35							
DRIVER				RECEIVER			
TDEC ₃	TDEC ₂	TDEC ₁	TDEC ₀	RDEC ₃	RDEC ₂	RDEC ₁	RDEC ₀
1	1	1	0	1	1	1	0



$\overline{\text{STEN}}$	ST	$\overline{\text{TTEN}}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 8. Mode Diagram — V.35

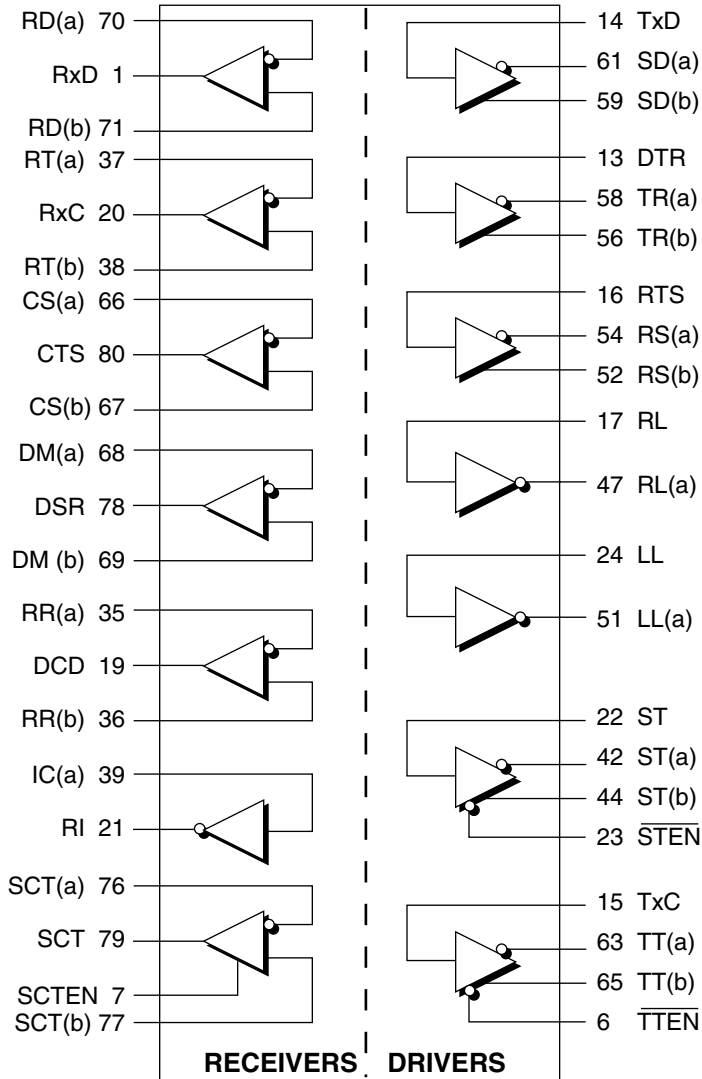
MODE: RS-422							
DRIVER				RECEIVER			
TDEC ₃	TDEC ₂	TDEC ₁	TDEC ₀	RDEC ₃	RDEC ₂	RDEC ₁	RDEC ₀
0	1	0	0	0	1	0	0



$\overline{\text{STEN}}$	ST	$\overline{\text{TTEN}}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 9. Mode Diagram — RS-422

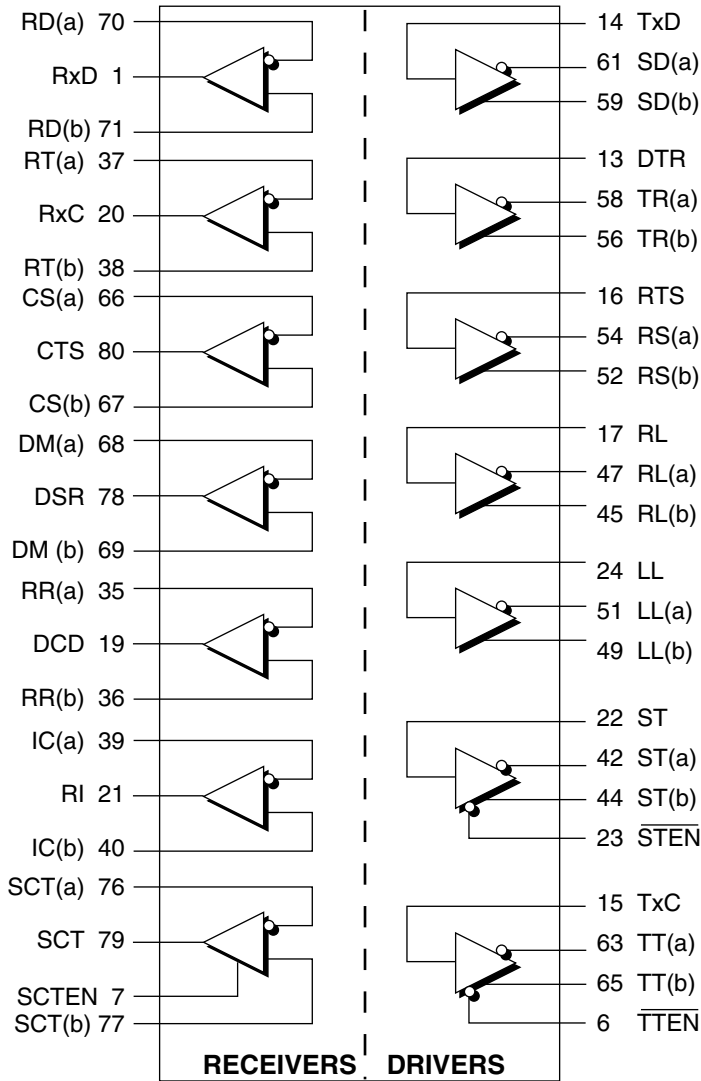
MODE: RS-449							
DRIVER				RECEIVER			
TDEC ₃	TDEC ₂	TDEC ₁	TDEC ₀	RDEC ₃	RDEC ₂	RDEC ₁	RDEC ₀
1	1	0	0	1	1	0	0



\overline{STEN}	ST	\overline{TTEN}	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 10. Mode Diagram — RS-449

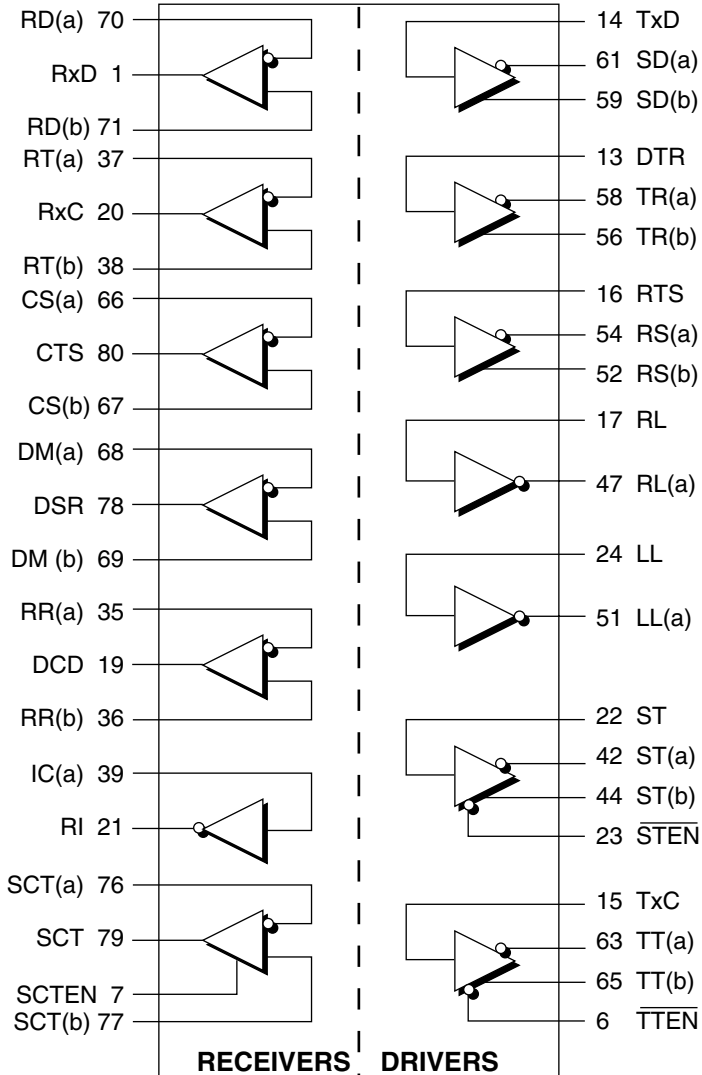
MODE: RS-485							
DRIVER				RECEIVER			
TDEC ₃	TDEC ₂	TDEC ₁	TDEC ₀	RDEC ₃	RDEC ₂	RDEC ₁	RDEC ₀
0	1	0	1	0	1	0	1



$\overline{\text{STEN}}$	ST	$\overline{\text{TTEN}}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 11. Mode Diagram — RS-485

MODE: EIA-530							
DRIVER				RECEIVER			
TDEC ₃	TDEC ₂	TDEC ₁	TDEC ₀	RDEC ₃	RDEC ₂	RDEC ₁	RDEC ₀
1	1	0	1	1	1	0	1



$\overline{\text{STEN}}$	ST	$\overline{\text{TTEN}}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 12. Mode Diagram — EIA-530

SP502/SP503 EVALUATION BOARD

The **SP502/SP503 Evaluation Board (EB)** is designed to offer as much flexibility to the user as possible. Each board comes equipped with an 80-pin QFP Zero-Insertion Force socket to allow for testing of multiple devices. The control lines and inputs and outputs of the device can be controlled either manually or via a data bus under software control. There is a 50-pin connector to allow for easy connection to an existing system via a ribbon cable. There are also open areas on the PC board to add additional circuitry to support application-specific requirements.

Manual Control

The **SP502/SP503EB** will support both the **SP502** or **SP503** multi-mode serial transceivers. When used for the **SP502**, disregard all notation on the board that is in [brackets]. The **SP502** has a half-duplex connection between the RxT receiver and the TT driver. Due to this internal connection, the RxT receiver inputs can be accessed via the TT(a) and TT(b) pins. If the user needs separate receiver input test pins, jumpers JP1 and JP2 can be inserted to allow for separate receiver inputs located at SCT(a) and SCT(b). The corresponding TTL output for this receiver is labeled as SCT. This test point is tied to pin 79 of the **SP502** or **SP503**. Pin 7 of the evaluation board is connected to the DIP switch, and is labeled as (SCTEN). When used with the **SP502**, this pin should be switched to a low state. When the evaluation board is used with the **SP503**, pin 7 is a tri-state control pin for the SCT receiver.

The transceiver I/O lines are brought out to test pins arranged in the same configuration as shown elsewhere in this data sheet. A top layer silk-screen shows the drivers and receivers to allow direct correlation to the data sheet. The transmitter and receiver decode bits are tied together and are brought out to a DIP switch for manual control of both the driver and receiver interface modes. Since the coding for the drivers and receivers is identical, the bits have been tied together. The DIP switch has 7 positions, four of which are reserved for the TDEC/RDEC control and the other three are used as tri-state control pins. The labels that are in [brackets] apply only

to the **SP503**. If a logic one is asserted, the corresponding red LED will be lit. If a zero is asserted, the corresponding red LED will not be lit.

Software Control

A 50-pin connector brings all the analog and digital I/O lines, V_{CC} , and GND to the edge of the card. This can be wired to the user's existing design via a ribbon cable. The pinout for the connector is described in the following section. When the evaluation board is operated under software control, the DIP switch should be set up so that all bits are LOW (all LEDs off). This will tie 20k Ω pulldown resistors from the inputs to ground and let the external system control the state of the control inputs.

Power and Ground Requirements

The evaluation board layout has been optimized for performance by using basic analog circuit techniques. The four charge-pump capacitors must be 22 μ F (16V) and be placed as close to the unit as possible; tantalum capacitors are suggested. The decoupling capacitor must be a minimum of 1 μ F; depending upon the operating environment, 10 μ F should be enough for worst case situations. The ground plane for the part must be solid, extending completely under the package. The power supplies for the device should be as accurate as possible; for rated performance $\pm 5\%$ is necessary. The power supply current will vary depending upon the selected mode, the amount of loading and the data rate. As a maximum, the user should reserve 200mA for I_{CC} . The worst-case operating mode is RS-485 under full load of six (6) drivers supplying 1.6V to 54 Ω loads. The power and ground inputs can be supplied through either the banana jacks on the evaluation board (Red = V_{CC} = $+5V \pm 5\%$; Black = GND) or through the connector.

For reference, the 80-pin QFP Socket is a TESCO part number FPQ-80-65-09A. The 50-pin connector is an AMP part number 749075-5.

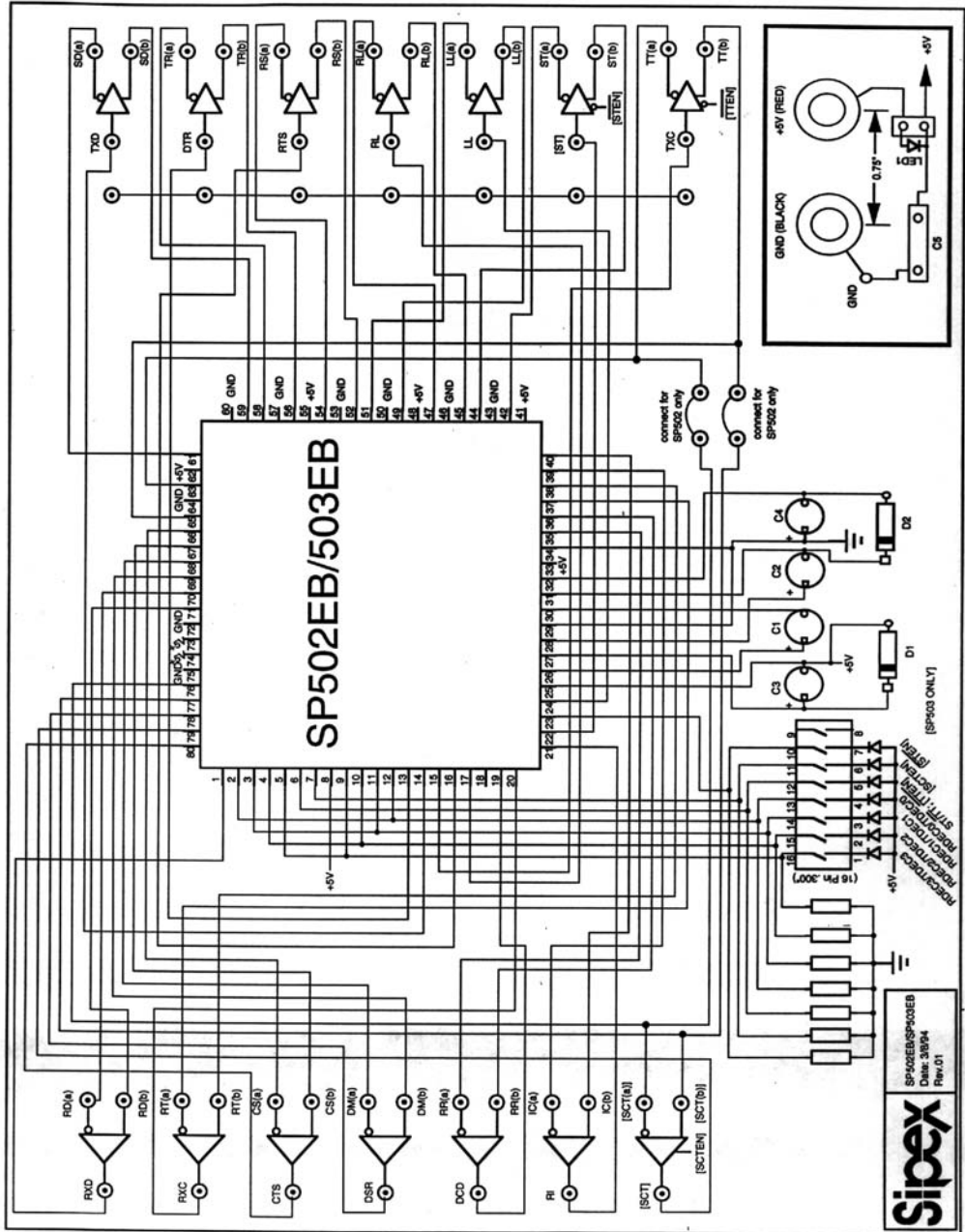


Figure 13. SP502/503 Evaluation Board Schematic

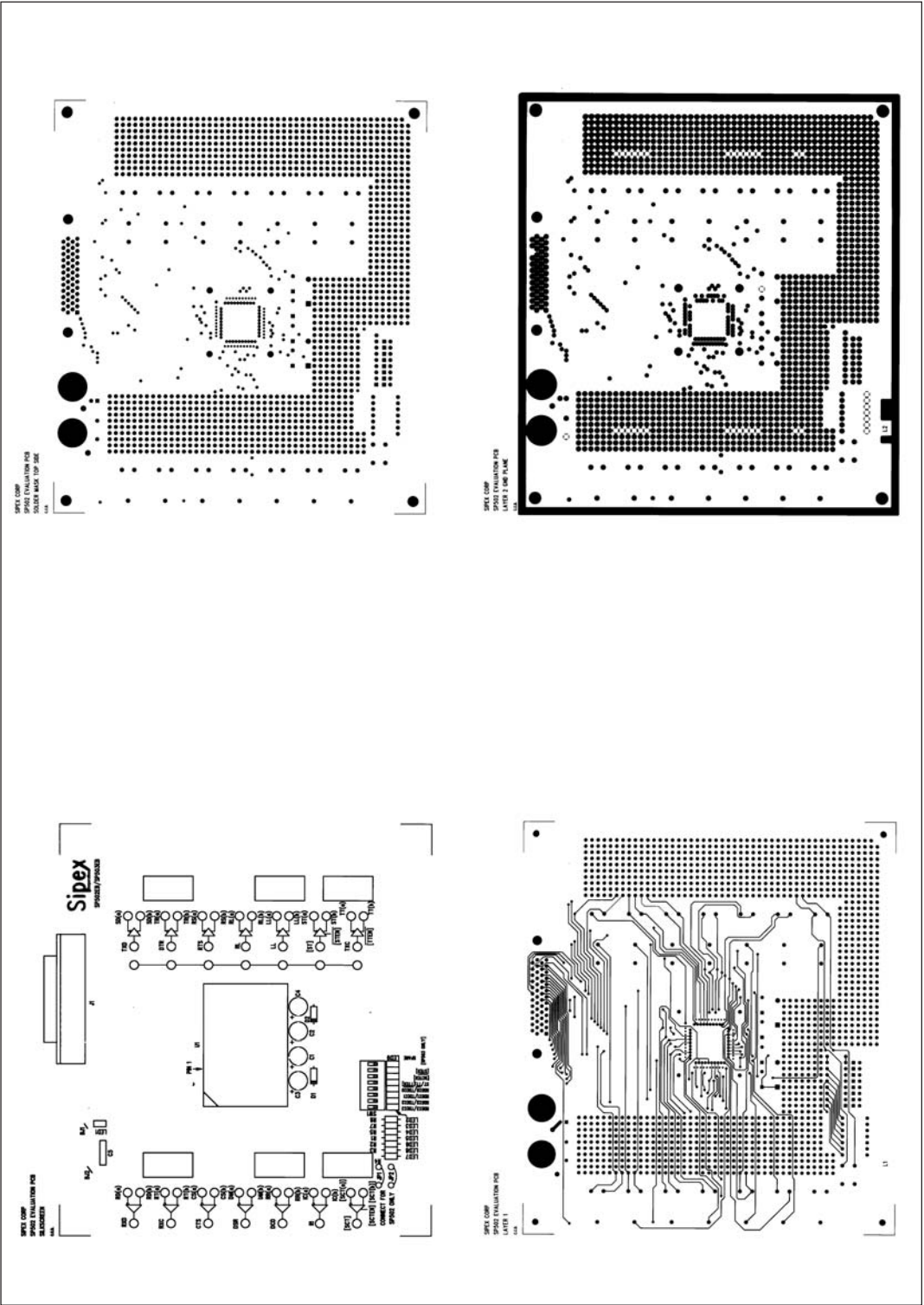


Figure 14a. Evaluation Board — Top Layers

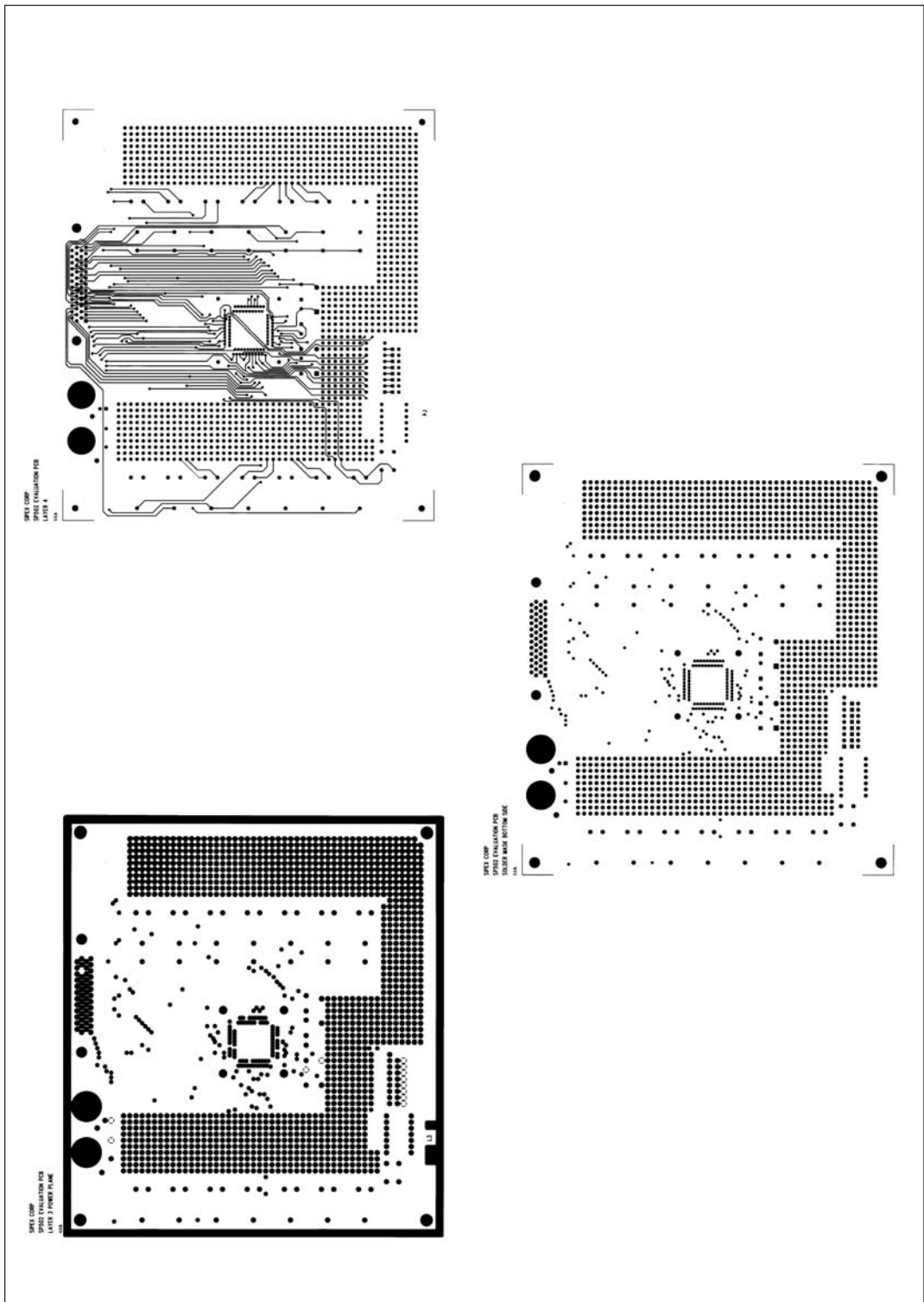
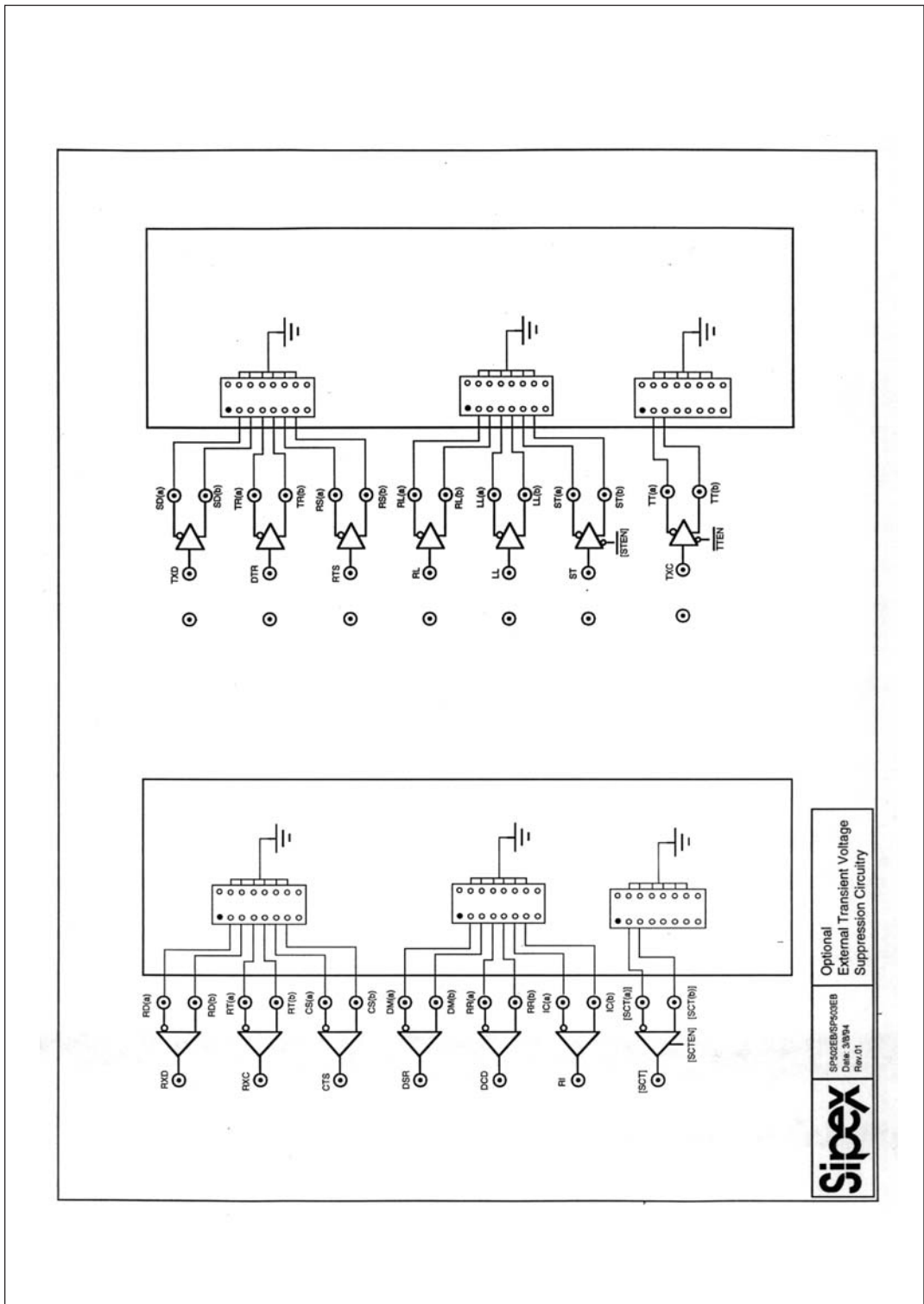


Figure 14b. Evaluation Board — Bottom Layers

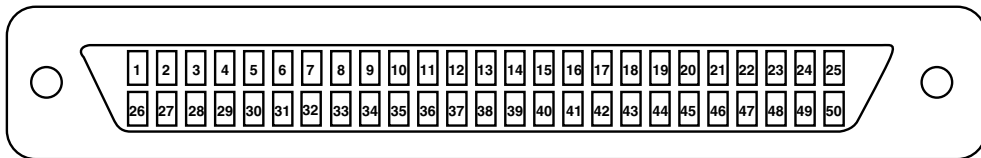


Optional
External Transient Voltage
Suppression Circuitry

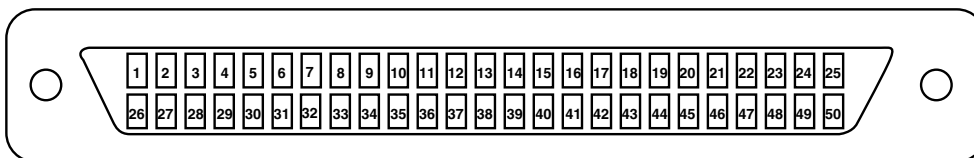
SP500ENSP500EB
Date: 3/2004
Rev: 01

Sipex

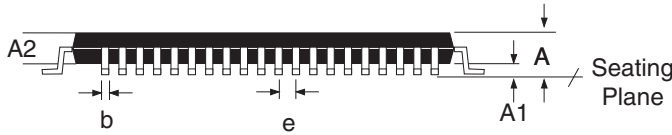
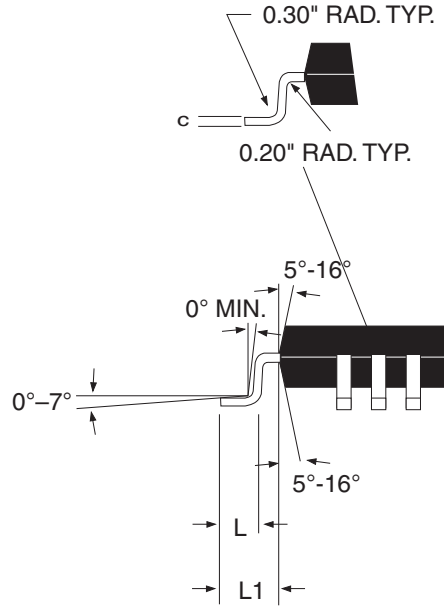
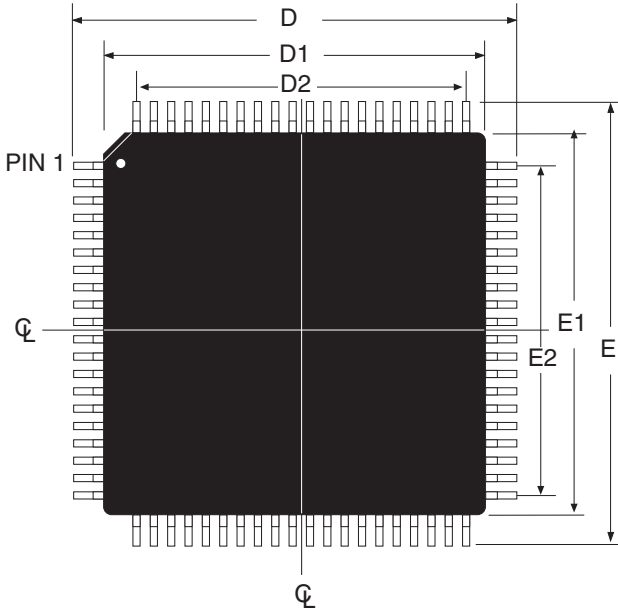
Figure 15. External Transient Suppressors



EDGE CONNECTOR	DUT PIN DESCRIPTIONS	EDGE CONNECTOR	DUT PIN DESCRIPTIONS
01	TxD (pin 14) –TTL Input – Transmit data; source for SD(a) and SD(b) outputs.	13	RD(a) (pin 70) – Analog In – Receive data, inverted: source for RxD.
02	DTR (pin 13) – TTL Input – Data terminal ready: source for TR(a) and TR(b) outputs.	14	DM(b) (pin 69) – Analog In – Data mode, non–inverted; source for DSR.
03	ST/ $\overline{\text{TT}}$ (pin 6) –TTL Input – ST/ $\overline{\text{TT}}$ select pin; enables ST drivers and disables TT drivers when high. Disables ST drivers and enables TT drivers when low.	15	DM(a) (pin 68) – Analog In – Data mode, inverted; source for DSR.
04	DEC ₃ /RDEC ₃ (pin 5) – TTL Input – Transmitter/Receiver decode register.	16	CS(b) (pin 67) – Analog In – Clear to send; non–inverted; source for CTS.
05	TDEC ₂ /RDEC ₂ (pin 4) – TTL Input – Transmitter/Receiver decode register.	17	CS(a) (pin 66) – Analog In – Clear to send, inverted; source for CTS.
06	TDEC ₁ /RDEC ₁ (pin 3) – TTL Input – Transmitter/Receiver decode register.	18	TT(b) (pin 65) – Analog Out – Terminal timing, non–inverted: sourced from TxC input.
07	TDEC ₀ /RDEC ₀ (pin 2) – TTL Input – Transmitter/Receiver decode register.	19	TT(a) (pin 63) – Analog Out – Terminal timing; inverted: sourced from TxC input.
08	RxD (pin 1) – TTL Output – Receive data; sourced from RD(a) and RD(b) inputs.	20	TR(a) (pin 58) – Analog Out – Terminal ready, inverted; sourced from DTR.
09	CTS (pin 80) – TTL Output – Clear to send; sourced from CS(a) and CS(b) inputs.	21	TR(b) (pin 56) – Analog Out – Terminal ready; non–inverted; sourced from DTR.
10	RxT (pin 79) – TTL Output – RxT; sourced from TT(a), TT(b) inputs.	22	SD(a) (pin 61) – Analog Out – Send data, inverted; sourced from TxD.
11	DSR (pin 78) – TTL Output – Data set ready; sourced from DM(a) and DM(b) inputs.	23	SD(b) (pin 59) – Analog Out – Send data; non–inverted; sourced from TxD.
12	RD(b) (pin 71) – Analog In – Receive data, non–inverted; source for RxD.	24	RS(a) (pin 54) – Analog Out – Ready to send; inverted; sourced from RTS.
		25	RS(b) (pin 52) – Analog Out – Ready to send, non–inverted; sourced from RTS.



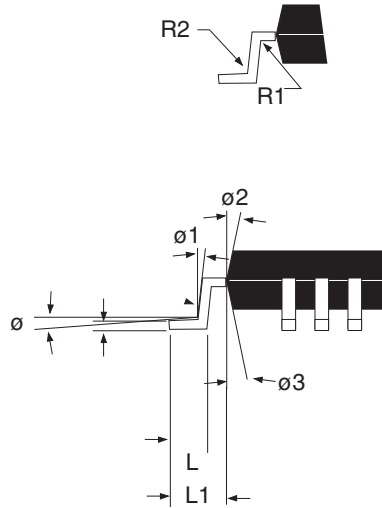
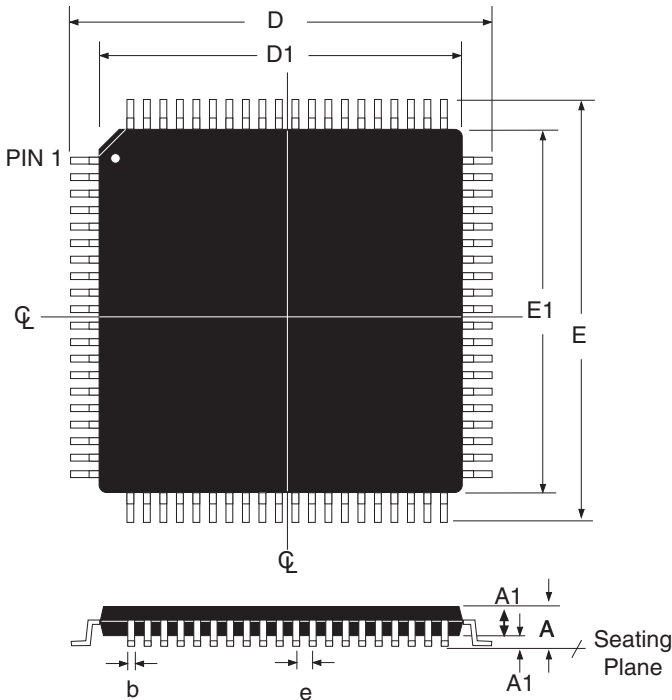
EDGE CONNECTOR	DUT PIN DESCRIPTIONS	EDGE CONNECTOR	DUT PIN DESCRIPTIONS
26	ST (pin 22) – TTL Input – Send Timing; source for ST(a) and ST(b) outputs. SP503 only.	39	IC(a) (pin 39) – Analog In – Incoming call; inverted; source for RI.
27	STEN (pin 23) – TTL Input — Driver enable control pin; active low. SP503 only,	40	RT(b) (pin 38) – Analog In – Receive timing, non–inverted; source for RxC.
28	SCT(a) (pin 76) – Analog Input – Inverting; input for SCT receiver; SP503 only.	41	RT(a) (pin 37) – Analog In – Receive timing; inverted; source from RxC.
29	SCT(b) (pin 77) – Analog Input – Non–inverting; input for SCT receiver. SP503 only.	42	RR(b) (pin 36) – Analog In – Receiver ready; non–inverted; source for DCD.
30	V _{CC} — +5V for all circuitry.	43	RR(a) (pin 35) – Analog In – Receiver ready; inverted; source for DCD.
31	GND — signal and power ground.	44	LL (pin 24) – TTL Input – Local loopback; source for LL(a) and LL(b) outputs.
32	LL(a) (pin 51) – Analog Out – Local loopback, inverted; sourced from LL.	45	RI (pin 21) – TTL Output – Ring indicator; sourced from IC(a) and IC(b) inputs.
33	LL(b) (pin 49) – Analog Out – Local loopback, non–inverted sourced from LL.	46	RxC (pin 20) – TTL Output – Receive clock; sourced from RT(a) and RT(b) inputs.
34	RL(a) (pin 47) – Analog Out – Remote loopback; inverted; sourced from RL.	47	DCD (pin 19) – TTL Output – Data carrier detect; sourced from RR(a) and RR(b) inputs.
35	RL(b) (pin 45) – Analog Out – Remote loopback; non–inverted; sourced from RL.	48	RL (pin 17) – Analog Out – Remote loopback; source for RL(a) and RL(b) outputs.
36	ST(b) (pin 44) – Analog Out – Send timing, non–inverted; sourced from TxC.	49	RTS (pin 16) – TTL Input – Ready to send; source for RS(a) and RS(b) outputs.
37	ST(a) (pin 42) – Analog Output – Send timing, inverted; sourced from TxC.	50	TxC (pin 15) – TTL Input – Transmit clock; source for TT(A) and TT(B) outputs.
38	IC(b) (pin 40) – Analog In – Incoming call; non–inverted; source for RI.		



DIMENSIONS Minimum/Maximum (mm)	80-PIN MQFP JEDEC MS-22 (BEC) Variation		
	MIN	NOM	MAX
A			2.45
A1	0.00		0.25
A2	1.80	2.00	2.20
b	0.22		0.40
D	17.20 BSC		
D1	14.00 BSC		
D2	12.35 REF		
E	17.20 BSC		
E1	14.00 BSC		
E2	12.35 REF		
e	0.65 BSC		
N	80		

COMMON DIMENSIONS			
SYMBL	MIN	NOM	MAX
c	0.11		23.00
L	0.73	0.88	1.03
L1	1.60 BASIC		

80 PIN MQFP (MS-022 BC)



DIMENSIONS Minimum/Maximum (mm)	80-PIN LQFP JEDEC MS-026 (BEC) Variation		
	MIN	NOM	MAX
A	1.40		1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
D	16.00 BSC		
D1	14.00 BSC		
e	0.65 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45		0.75
L1	1.00 REF		
ø	0°	3.5°	7°
ø1	0°	-	-
ø2	11°	12°	13°
ø3	11°	12°	13°
R1	0.08	-	-
R2	0.08	-	0.20

80 PIN LQFP

ORDERING INFORMATION

Part Number	Top Mark	Temperature Range	Package Types
SP503CF	SP503CFYYWW	0°C to +70°C	80-pin JEDEC (MS-022 BC) MQFP
SP503EF	SP503EFYYWW	-40°C to +85°C	80-pin JEDEC (MS-022 BC) MQFP
SP503EM	SP503EMYYWW	-40°C to +85°C	80-pin JEDEC (MS-022 BC) LQFP

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP503EF = standard; SP503EF-L = lead free

REVISION HISTORY

DATE	REVISION	DESCRIPTION
1/27/04	A	Implemented tracking revision.
5/6/04	B	Added Top Mark to ordering information.
7/29/04	C	Included LQFP package option.



ANALOG EXCELLENCE

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