

128K x 8 LOW POWER CMOS STATIC RAM

DECEMBER 2003

FEATURES

- High-speed access time: 35, 70 ns
- Low active power: 450 mW (typical)
- Low standby power: 150 μ W (typical) CMOS standby
- Output Enable (\overline{OE}) and two Chip Enable ($\overline{CE1}$ and $\overline{CE2}$) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V ($\pm 10\%$) power supply

DESCRIPTION

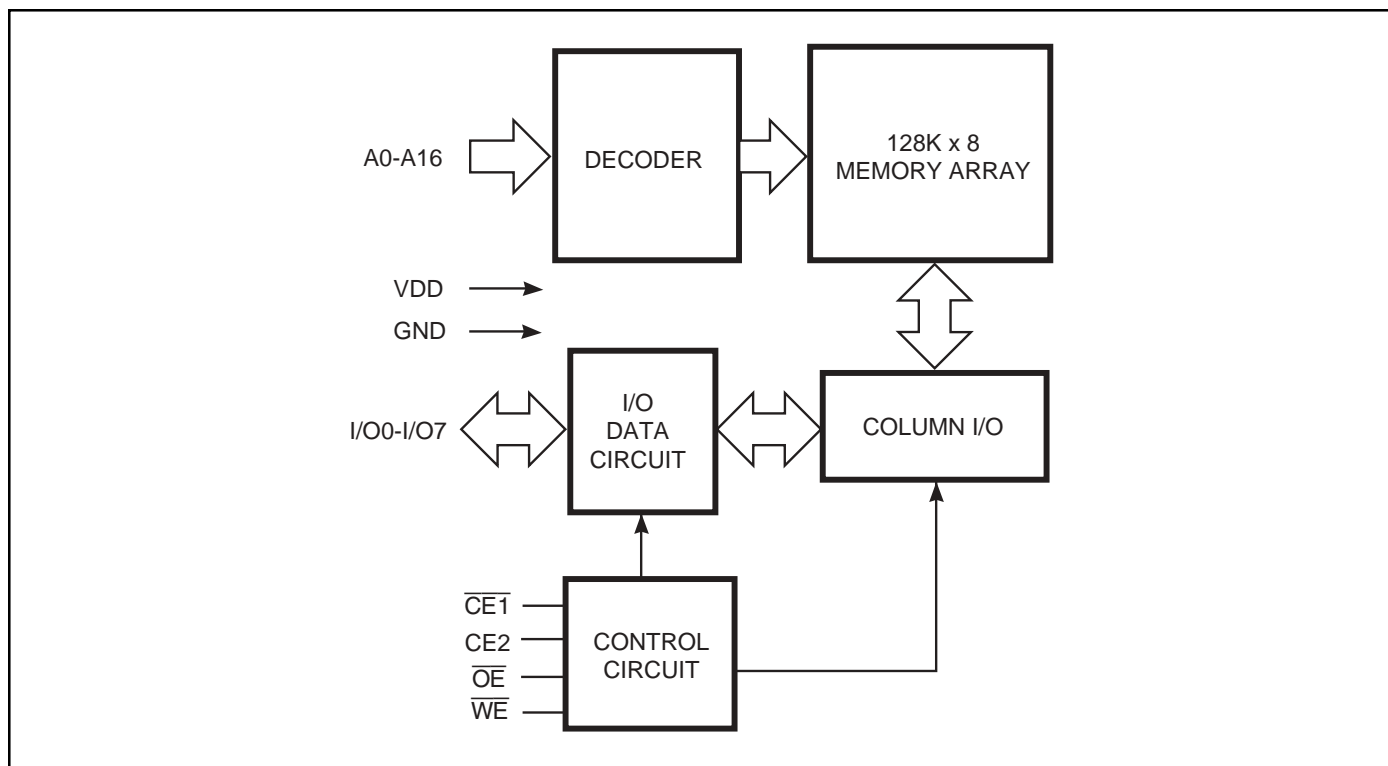
The *ISSI* IS62C1024L is a low power, 131,072-word by 8-bit CMOS static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or $\overline{CE2}$ is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and $\overline{CE2}$. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS62C1024L is available in 32-pin plastic SOP and TSOP (type 1) packages.

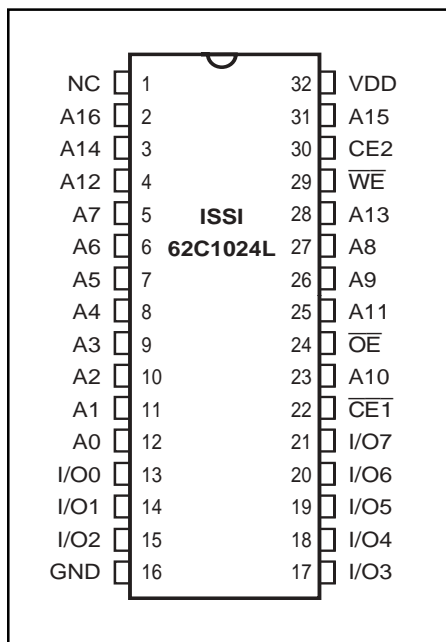
FUNCTIONAL BLOCK DIAGRAM



Copyright © 2003 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

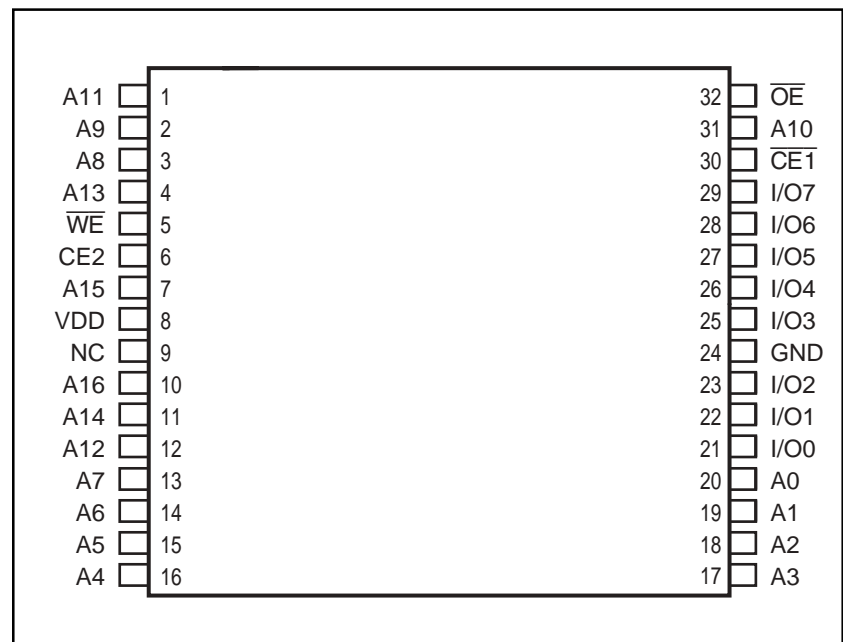
PIN CONFIGURATION

32-Pin SOP



PIN CONFIGURATION

32-Pin TSOP (Type 1)



PIN DESCRIPTIONS

| | |
|------------------|---------------------|
| A0-A16 | Address Inputs |
| $\overline{CE1}$ | Chip Enable 1 Input |
| CE2 | Chip Enable 2 Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| V _{DD} | Power |
| GND | Ground |

OPERATING RANGE

| Range | Ambient Temperature | V _{DD} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | -40°C to +85°C | 5V ± 10% |

TRUTH TABLE

| Mode | \overline{WE} | $\overline{CE1}$ | CE2 | \overline{OE} | I/O Operation | V _{DD} Current |
|-----------------|-----------------|------------------|-----|-----------------|------------------|-------------------------------------|
| Not Selected | X | H | X | X | High-Z | I _{SB1} , I _{SB2} |
| (Power-down) | X | X | L | X | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | H | L | H | H | High-Z | I _{CC} |
| Read | H | L | H | L | D _{OUT} | I _{CC} |
| Write | L | L | H | X | D _{IN} | I _{CC} |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|--------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.5 | W |
| I _{OUT} | DC Output Current (LOW) | 20 | mA |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|----------------------------------|---|--------------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -1.0 mA | 2.4 | — | V |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 2.1 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{DD} + 0.5 | V |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | Com. Ind. | -2 10 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} | Com. Ind. | -2 10 | μA |

Notes:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -35 ns | | -70 ns | | Unit |
|------------------|--|---|------|--------|------|--------|------|------|
| | | | | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = f _{MAX} | Com. | — | 100 | — | 70 | mA |
| | | | Ind. | — | 110 | — | 80 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} , $\overline{CE1} \geq V_{IH}$, or CE2 ≤ V _{IL} , f = 0 | Com. | — | 10 | — | 10 | mA |
| | | | Ind. | — | 15 | — | 15 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., $\overline{CE1} \leq V_{DD} - 0.2V$, CE2 ≤ 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 500 | — | 500 | μA |
| | | | Ind. | — | 750 | — | 750 | |

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -35 | | -70 | | Unit |
|-----------------------------------|--|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 35 | — | 70 | — | ns |
| t _{AA} | Address Access Time | — | 35 | — | 70 | ns |
| t _{OHA} | Output Hold Time | 3 | — | 3 | — | ns |
| t _{ACE1} | $\overline{CE1}$ Access Time | — | 35 | — | 70 | ns |
| t _{ACE2} | CE2 Access Time | — | 35 | — | 70 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 10 | — | 35 | ns |
| t _{LZOE} ⁽²⁾ | \overline{OE} to Low-Z Output | 0 | — | 0 | — | ns |
| t _{HZOE} ⁽²⁾ | \overline{OE} to High-Z Output | 0 | 10 | 0 | 25 | ns |
| t _{LZCE1} ⁽²⁾ | $\overline{CE1}$ to Low-Z Output | 3 | — | 10 | — | ns |
| t _{LZCE2} ⁽²⁾ | CE2 to Low-Z Output | 3 | — | 10 | — | ns |
| t _{HZCE} ⁽²⁾ | $\overline{CE1}$ or CE2 to High-Z Output | 0 | 10 | 0 | 25 | ns |

Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
- Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

| Parameter | Unit |
|---|-----------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1a and 1b |

AC TEST LOADS

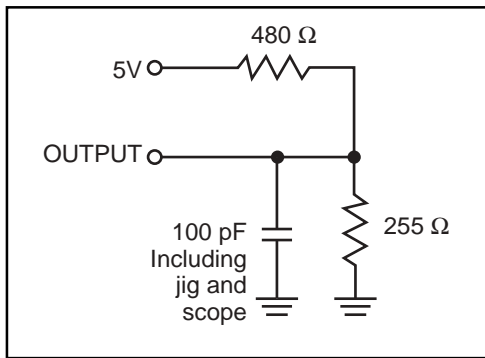


Figure 1a.

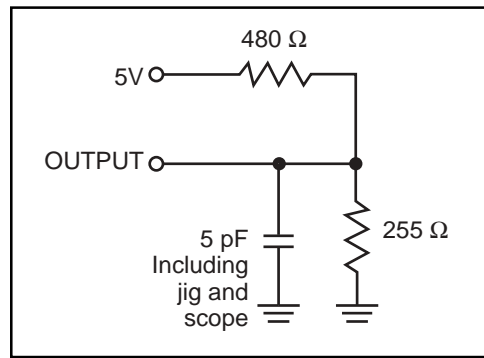
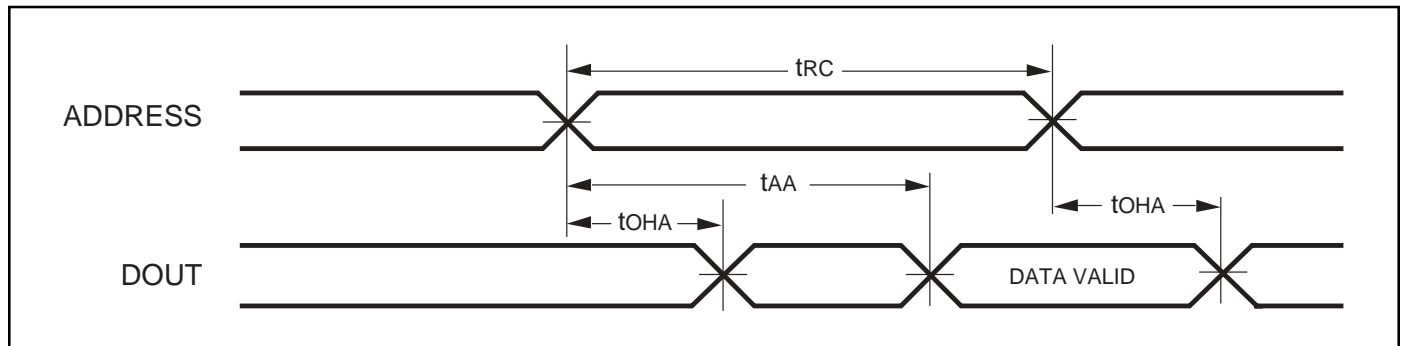
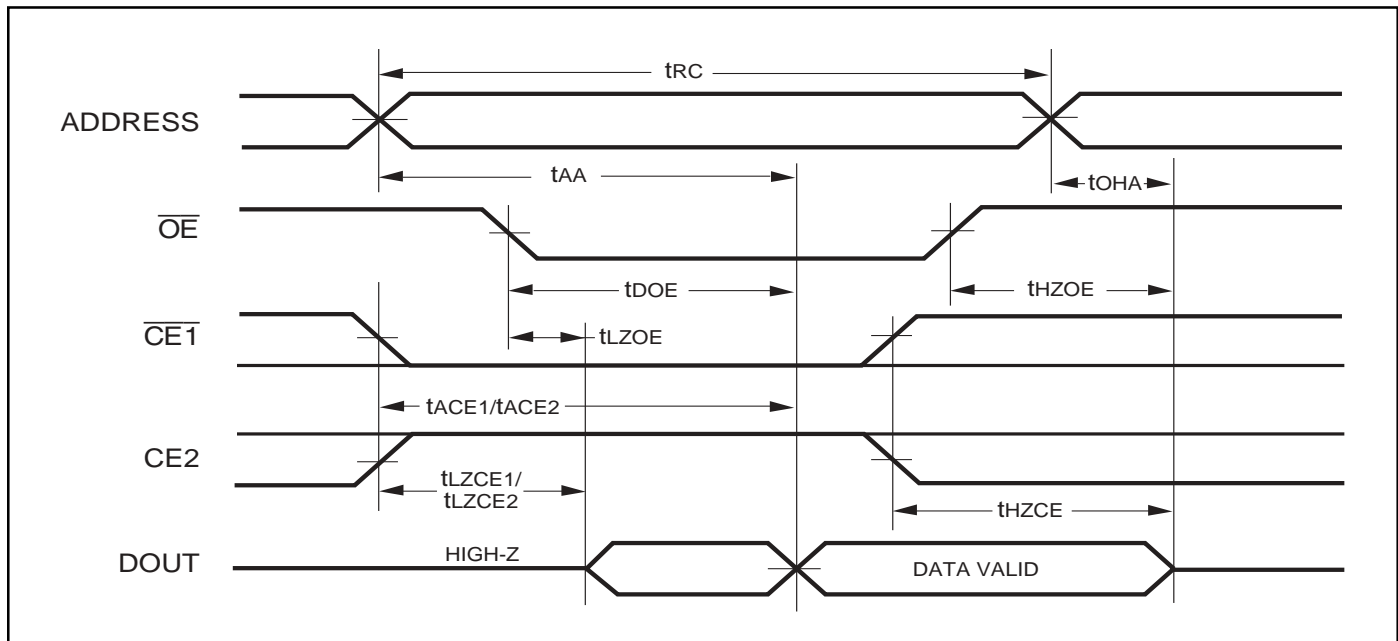


Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)**Notes:**

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and $CE2$ HIGH transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range, Standard and Low Power)

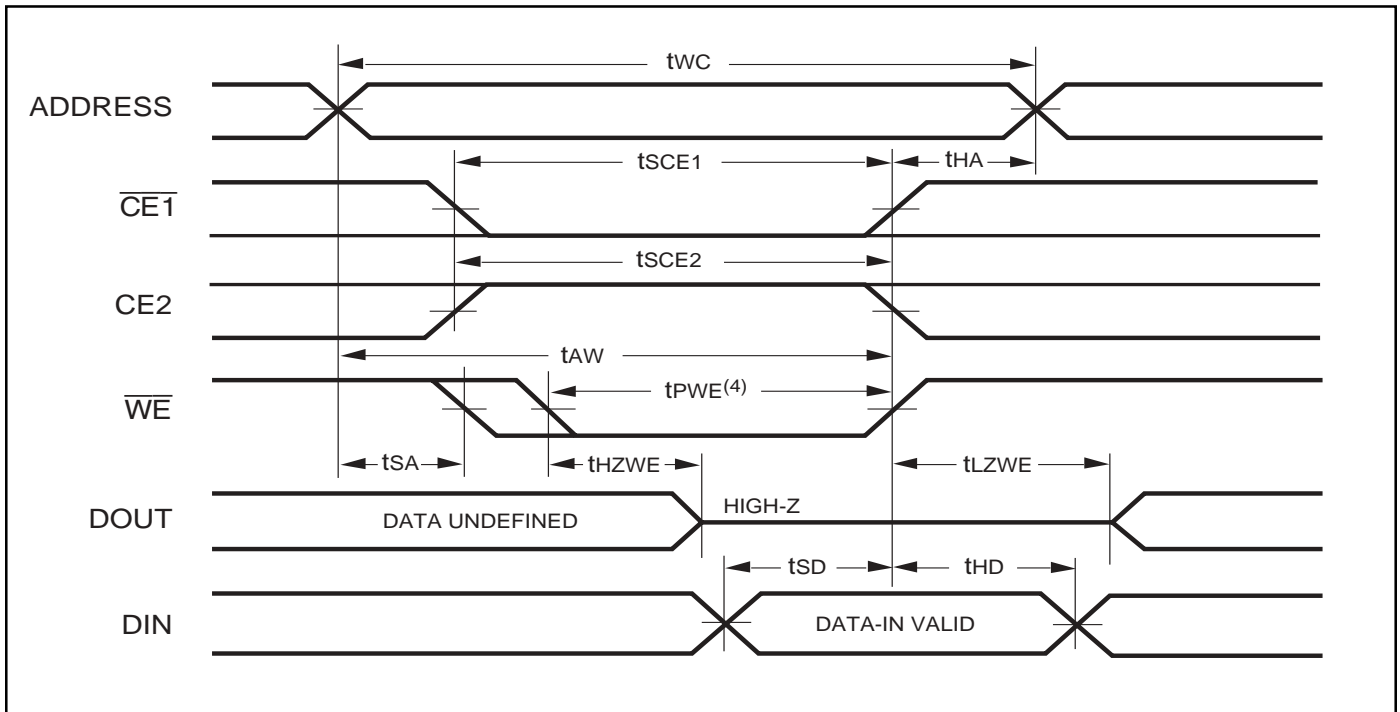
| Symbol | Parameter | -35 | | -70 | | Unit |
|------------------|--------------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t_{WC} | Write Cycle Time | 35 | — | 70 | — | ns |
| t_{SCE1} | $\overline{CE1}$ to Write End | 25 | — | 60 | — | ns |
| t_{SCE2} | $CE2$ to Write End | 25 | — | 60 | — | ns |
| t_{AW} | Address Setup Time to Write End | 25 | — | 60 | — | ns |
| t_{HA} | Address Hold from Write End | 0 | — | 0 | — | ns |
| t_{SA} | Address Setup Time | 0 | — | 0 | — | ns |
| $t_{PWE}^{(4)}$ | \overline{WE} Pulse Width | 25 | — | 50 | — | ns |
| t_{SD} | Data Setup to Write End | 20 | — | 30 | — | ns |
| t_{HD} | Data Hold from Write End | 0 | — | 0 | — | ns |
| $t_{HZWE}^{(2)}$ | \overline{WE} LOW to High-Z Output | — | 10 | — | 25 | ns |
| $t_{LZWE}^{(2)}$ | \overline{WE} HIGH to Low-Z Output | 3 | — | 5 | — | ns |

Notes:

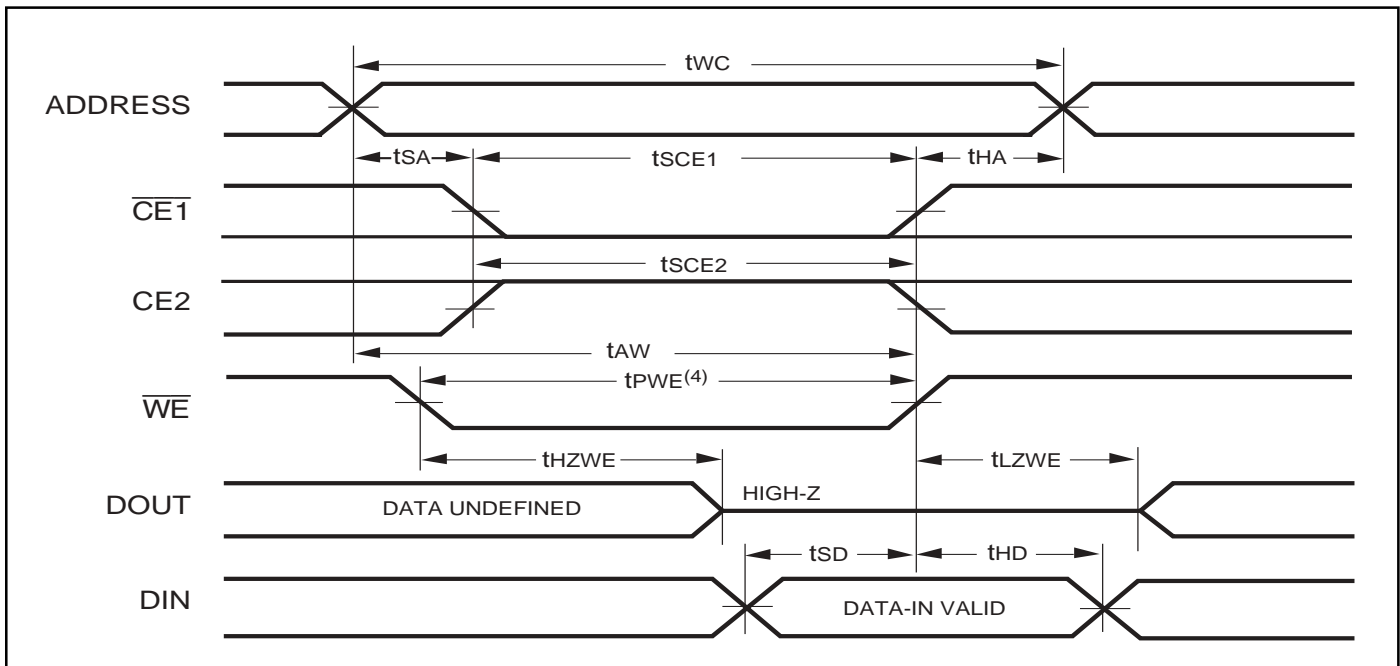
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, $CE2$ HIGH and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with \overline{OE} HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 (\overline{WE} Controlled)^(1,2)



WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 Controlled)^(1,2)



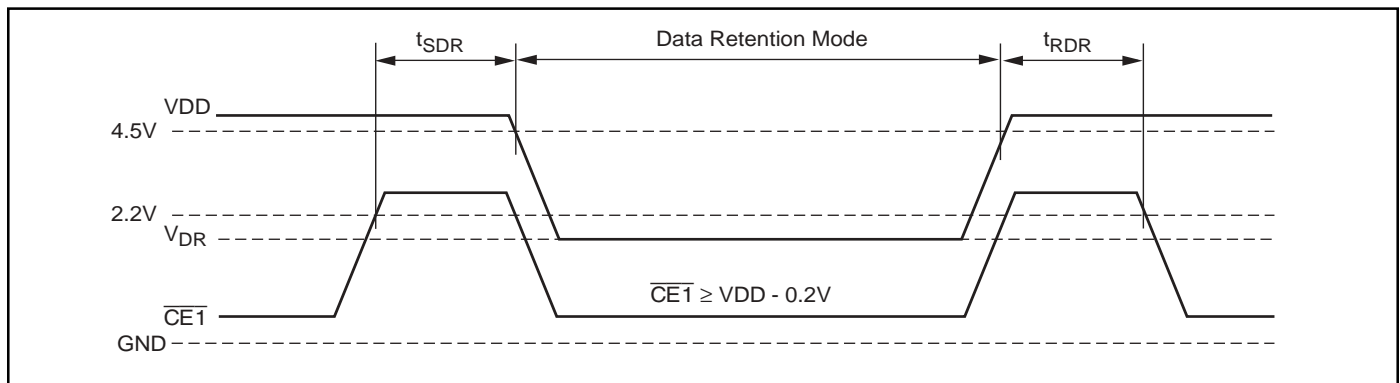
Notes:

1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} = V_{IH}$.

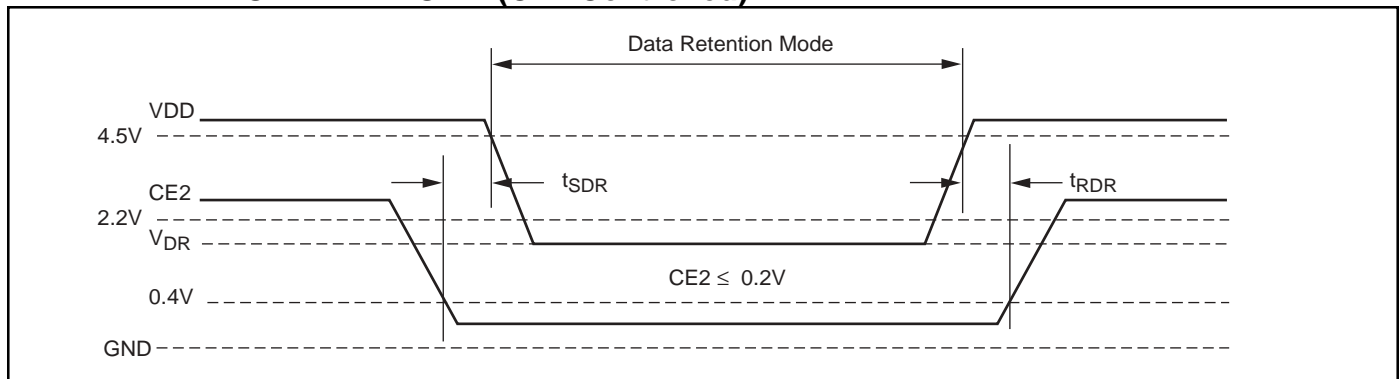
DATA RETENTION SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|------------------|------------------------------------|---|-----------------|----------|------------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | 2.0 | | 5.5 | V |
| I _{DR} | Data Retention Current | V _{DD} = 3.0V, $\overline{CE1} \geq V_{DD} - 0.2V$ | Com. Ind. | 45 60 | 250 400 | μA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | 0 | | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | t _{rc} | | — | ns |

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



DATA RETENTION WAVEFORM (CE2 Controlled)



ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

| Speed (ns) | Order Part No. | Package |
|------------|----------------|--------------|
| 35 | IS62C1024L-35Q | Plastic SOP |
| 35 | IS62C1024L-35T | TSOP, Type 1 |
| 70 | IS62C1024L-70Q | Plastic SOP |
| 70 | IS62C1024L-70T | TSOP, Type 1 |

Industrial Range: -40°C to +85°C

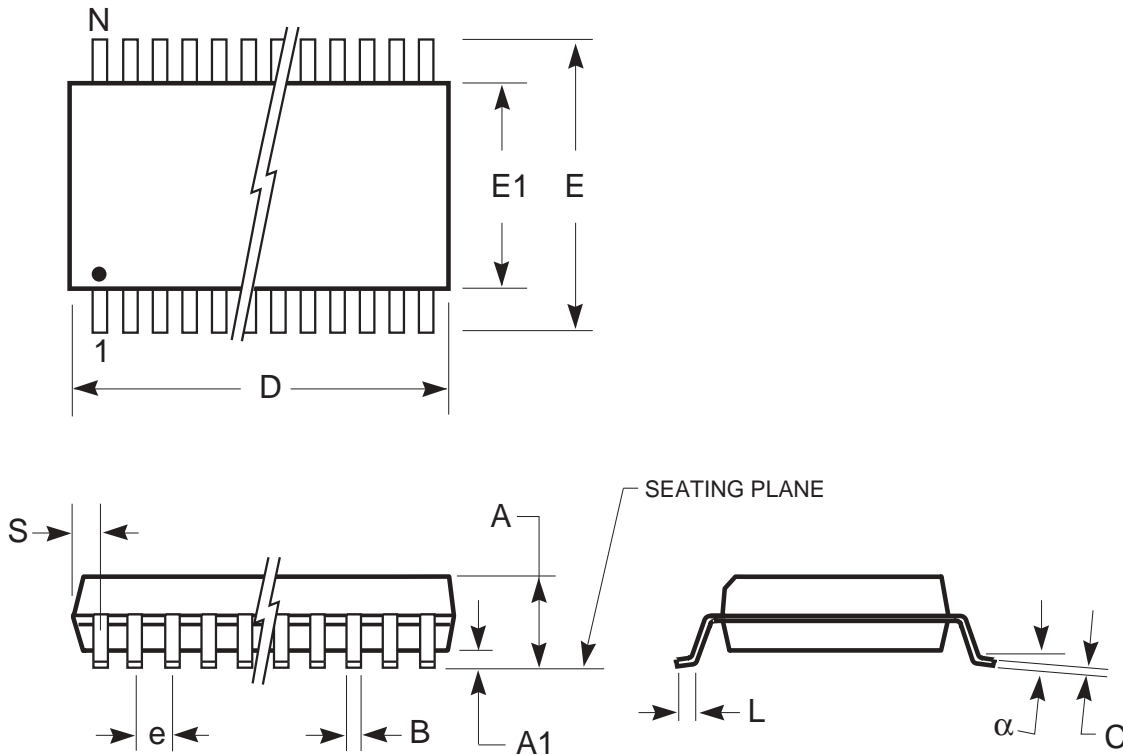
| Speed (ns) | Order Part No. | Package |
|------------|-----------------|--------------|
| 35 | IS62C1024L-35QI | Plastic SOP |
| 35 | IS62C1024L-35TI | TSOP, Type 1 |
| 70 | IS62C1024L-70QI | Plastic SOP |
| 70 | IS62C1024L-70TI | TSOP, Type 1 |

ISSI[®]***Integrated Silicon Solution, Inc.***

2231 Lawson Lane
Santa Clara, CA 95054
Tel: 1-800-379-4774
Fax: (408) 588-0806
E-mail: sales@issi.com
www.issi.com

PACKAGING INFORMATION

450-mil Plastic SOP
 Package Code: Q (32-pin)



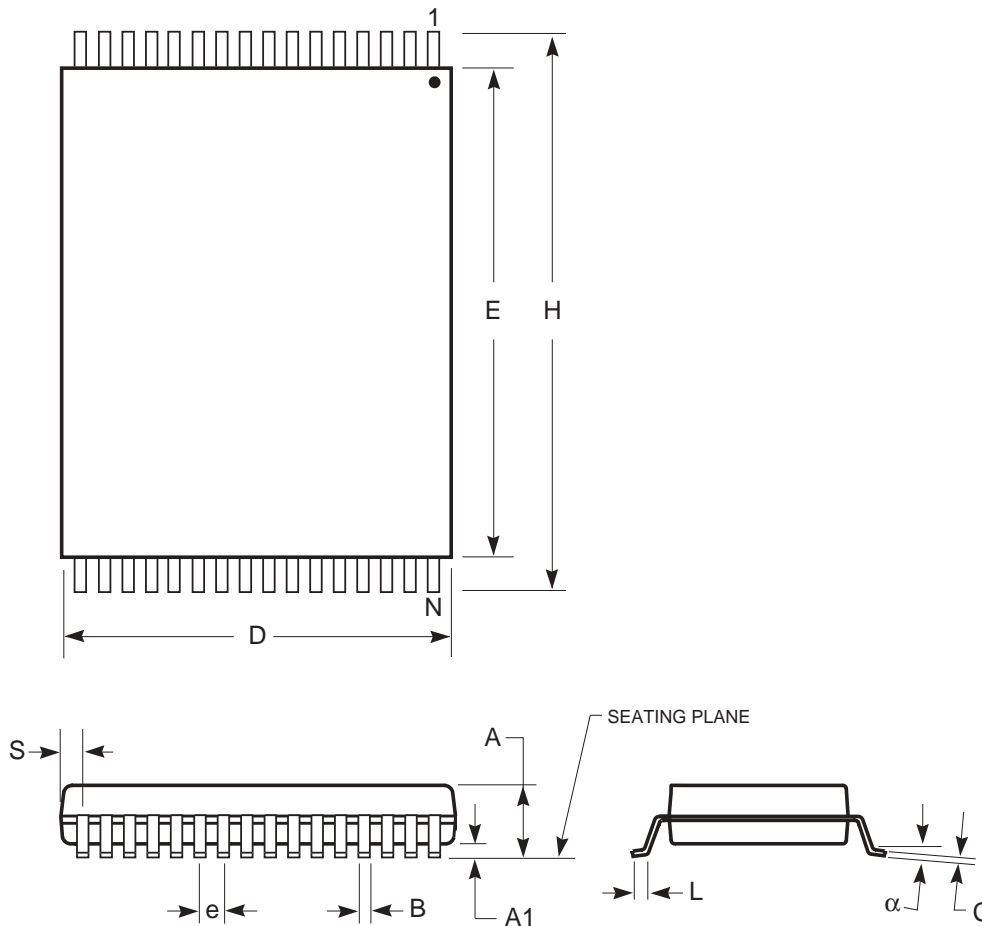
| | MILLIMETERS | | INCHES | |
|-----------|-------------|-------|-----------|-------|
| Symbol | Min. | Max. | Min. | Max. |
| No. Leads | 32 | | | |
| A | — | 3.00 | — | 0.118 |
| A1 | 0.10 | — | 0.004 | — |
| B | 0.36 | 0.51 | 0.014 | 0.020 |
| C | 0.15 | 0.30 | 0.006 | 0.012 |
| D | 20.14 | 20.75 | 0.793 | 0.817 |
| E | 13.87 | 14.38 | 0.546 | 0.566 |
| E1 | 11.18 | 11.43 | 0.440 | 0.450 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 0.58 | 0.99 | 0.023 | 0.039 |
| α | 0° | 10° | 0° | 10° |
| S | — | 0.86 | — | 0.034 |

Notes:

1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

Plastic TSOP-Type I
 Package Code: T (32-pin)



| | MILLIMETERS | | INCHES | |
|-----------|-------------|-------|-----------|-------|
| Symbol | Min. | Max. | Min. | Max. |
| No. Leads | 32 | | | |
| A | — | 1.20 | — | 0.047 |
| A1 | 0.05 | 0.25 | 0.002 | 0.010 |
| B | 0.17 | 0.23 | 0.007 | 0.009 |
| C | 0.12 | 0.17 | 0.005 | 0.007 |
| D | 7.90 | 8.10 | 0.311 | 0.319 |
| E | 18.30 | 18.50 | 0.720 | 0.728 |
| H | 19.80 | 20.20 | 0.780 | 0.795 |
| e | 0.50 BSC | | 0.020 BSC | |
| L | 0.40 | 0.60 | 0.016 | 0.024 |
| alpha | 0° | 8° | 0° | 8° |
| S | 0.25 REF | | 0.010 REF | |

Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Copyright © 2003 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.